

Features

- CMTI: 100 kV/ μs
- Input Voltage Range: $\pm 250\text{ mV}$ or $\pm 50\text{ mV}$
- Very Low Offset Error: 150 μV or 50 μV at 25°C (Max)
- Very Low Gain Error:
 - 0.3% at 25°C (Max) for TPA8101
 - 0.3% at 25°C (Max) for TPA8102
- System-Level Diagnostic Features
- Wide Temperature Range: -40°C to $+125^{\circ}\text{C}$
- TPA8101-SOAR-S is Qualified for Automotive Applications with the AEC-Q100 Reliability Test
- Finished Safety-Related Certifications:
 - CQC Certification per GB 4943.1
 - CB Certifications
 - 5000- V_{RMS} Isolation Rating per UL 1577
 - CSA, TUV Certifications
 - VDE Certification According to DIN VDE V 0884-17 (IEC60747-17)

Applications

- Industrial Automation
- Motor Control
- Power Supplies

Description

The device is a precision, delta-sigma modulator with an output separated from the input circuitry by a capacitive silicon dioxide insulation barrier. This barrier of the WSOP8 package is certified to provide isolation of up to 5000 V_{RMS} according to UL 1577.

The common-mode transient immunity (CMTI) of the device is significantly enhanced through innovative circuit design and optimized structure.

The input of the device is designed to connect to shunt resistors or other low-voltage level signal sources. The excellent performance of the device supports accurate current control in motor control applications. The common-mode overvoltage and missing high-side supply voltage detection feature system-level diagnostics. TPA8101-DG5R and TPA8102-DG5R with a small package size are designed for high accuracy, isolated current sensing in space constrained applications.

The device is available in the WSOP8, WSOP16, TSSOP8, and DFN2.7X3.5-8 packages, and is characterized from -40°C to $+125^{\circ}\text{C}$.

Quick Selection Guide:

Product	Input Range	Clock Type
TPA8101	$\pm 250\text{ mV}$	Clock In
TPA8102	$\pm 50\text{ mV}$	Clock In

Typical Application Circuit

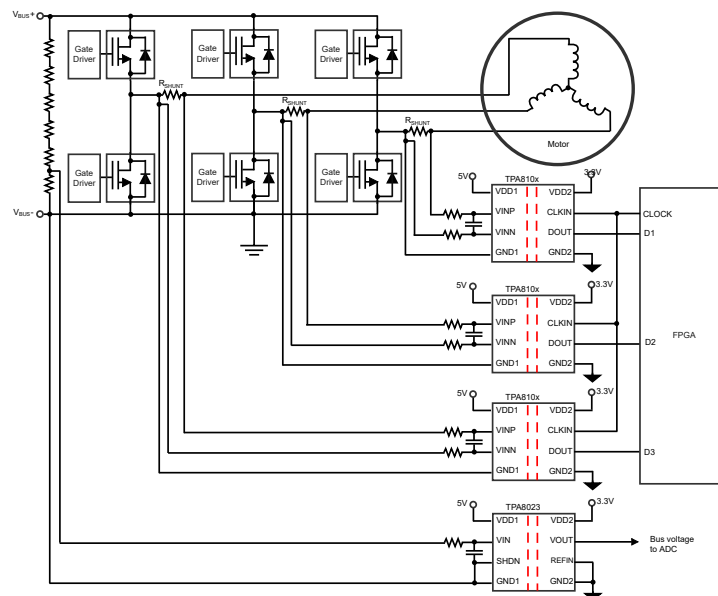


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Revision History

Date	Revision	Notes
2023-09-29	Rev.A.0	Initial version.
2024-12-18	Rev.A.1	Added new part numbers: TPA8101-SOBR and TPA8101-SOAR-S. Updated Safety-Related certificates number. Updated the Order Information. Updated the Tape and Reel Information.
2025-06-09	Rev.A.2	Added new part number: TPA8102-SOAR and related specifications. Added Sinc ³ filter test conditions of Typical Performance Characteristics. Added quick selection guide. Updated the POD format of the WSOP8. Updated the Insulation Specifications of TSSOP8 package. Changed the Maximum Gain Error specification of TPA8102 from " $\pm 0.15\%$ " to " $\pm 0.3\%$ ". Updated the AC PSRR, THD, SNR, SINAD and SFDR specifications of TPA8102.
2025-09-03	Rev.A.3	Added the digital interface timing of TPA8101 and TPA8102. Changed the Maximum Gain Error specification of the TPA8101 from " $\pm 0.15\%$ " to " $\pm 0.3\%$ ". Updated the status of the VDE certificate. The actual product remains unchanged.
2026-06-23	Rev.A.4	Added new part numbers: TPA8101-DG5R / TPA8102-DG5R and related specifications. Changed the typical R_{IN} of the TPA8102 from "19 k Ω " to "4.75 k Ω " and the typical R_{IND} of the TPA8102 from "22 k Ω " to "4.9 k Ω ". Added new figures of TPA8101 and TPA8102. Updated the Tape and Reel Information of TPA8101-TS1R. The actual product remains unchanged.

Pin Configuration and Functions

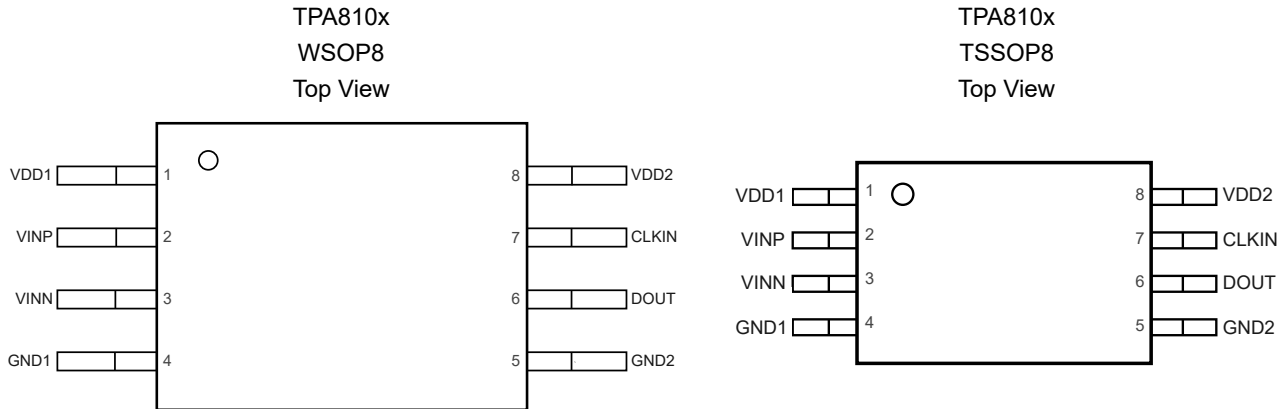
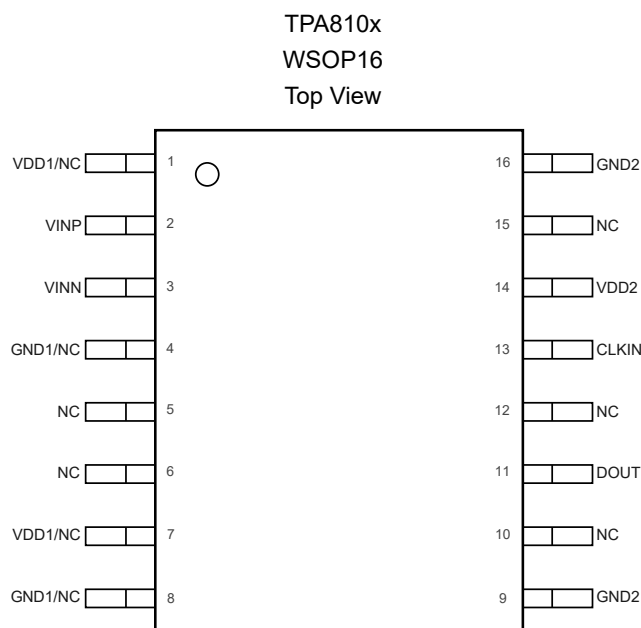
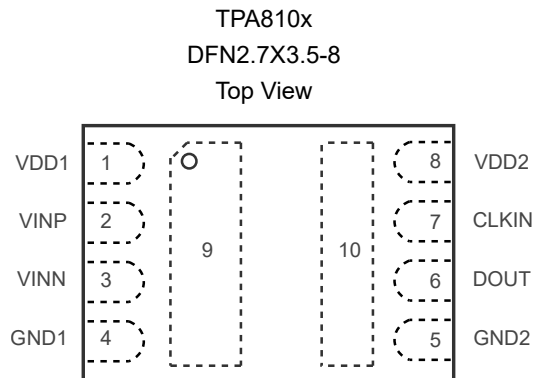


Table 1. Pin Functions

Pin		I/O	Description
No.	Name		
1	VDD1		High-side power supply.
2	VINP	I	Positive analog input.
3	VINN	I	Negative analog input.
4	GND1		High-side analog ground.
5	GND2		Low-side analog ground.
6	DOUT	O	Modulator data output.
7	CLKIN	I	Modulator clock input.
8	VDD2		Low-side power supply.

$\pm 250\text{-mV}$ or $\pm 50\text{-mV}$ Input Isolated Delta-Sigma Modulators

Table 2. Pin Functions

Pin		I/O	Description
No.	Name		
1	VDD1/NC		One of the Pin1 or Pin7 needs to be connected to the high-side power supply, and the other pin can be connected to the high-side power supply or left float.
2	VINP	I	Positive analog input.
3	VINN	I	Negative analog input.
4	GND1/NC		One of the Pin4 or Pin8 needs to be connected to the high-side analog ground, and the other pin can be connected to the high-side analog ground or left float.
5	NC		Not connect.
6	NC		Not connect.
7	VDD1/NC		One of the Pin1 or Pin7 needs to be connected to the high-side power supply, and the other pin can be connected to the high-side power supply or left float.
8	GND1/NC		One of the Pin4 or Pin8 needs to be connected to the high-side analog ground, and the other pin can be connected to the high-side analog ground or left float.
9	GND2		Low-side analog ground.
10	NC		Not connect.
11	DOUT	O	Modulator data output.
12	NC		Not connect.
13	CLKIN	I	Modulator clock input.
14	VDD2		Low-side power supply.
15	NC		Not connect.
16	GND2		Low-side analog ground.

$\pm 250\text{-mV}$ or $\pm 50\text{-mV}$ Input Isolated Delta-Sigma Modulators

Table 3. Pin Functions

Pin		I/O	Description
No.	Name		
1	VDD1		High-side power supply.
2	VINP	I	Positive analog input.
3	VINN	I	Negative analog input.
4, 9	GND1		High-side analog ground.
5, 10	GND2		Low-side analog ground.
6	DOUT	O	Modulator data output.
7	CLKIN	I	Modulator clock input.
8	VDD2		Low-side power supply.

±250-mV or ±50-mV Input Isolated Delta-Sigma Modulators

Specifications

Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter	Min	Max	Unit
V _{DD}	Supply Voltage, VDD1 to GND1 or VDD2 to GND2	-0.3	7	V
V _{INPUT}	Analog Input Voltage at VINP, VINN	GND1 – 6	VDD1 + 0.5	V
	Digital Input or Output Voltage at CLKIN, DOUT	GND1 – 0.5	VDD2 + 0.5	V
I _{IN}	Input Current to Any Pin except Supply Pins	-10	10	mA
T _J	Operating Virtual Junction Temperature		150	°C
T _{STG}	Storage Temperature Range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V _{DD1}	High-Side Supply Voltage (VDD1 to GND1)	3.0	5.0	5.5	V
V _{DD2}	Low-Side Supply Voltage (VDD2 to GND2)	3.0	3.3	5.5	V
T _A	Operating Ambient Temperature	−40	25	125	°C

Thermal Information

Package Type	θ _{JA}	θ _{JC}	Unit
WSOP8	85	43	°C/W
TSSOP8	191	44	°C/W
WSOP16	83	41	°C/W
DFN2.7X3.5-8	39.5	69.1	°C/W

Insulation Specifications

The value of UL and VDE is provided by lab test, and the UL and VDE certifications are ongoing.

Parameter		Conditions	Value		Unit
			WSOP8	TSSOP8	
CLR	External Clearance	Shortest terminal-to-terminal distance through air	8.0	4.0	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	8.0	4.0	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	22	22	μm
DTC	Distance through the Molding Compound	Minimum internal distance across the conductors inside the package	0.8	0.8	mm
CTI	Comparative Tracking Index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	> 600	> 600	V
	Material Group	According to IEC 60664-1	I	I	
	Over-Voltage Category	For Rated Mains Voltage ≤ 150 V _{RMS}	I-IV	I-IV	
		For Rated Mains Voltage ≤ 300 V _{RMS}	I-IV	I-III	
		For Rated Mains Voltage ≤ 600 V _{RMS}	I-IV	I-II	
		For Rated Mains Voltage ≤ 1000 V _{RMS}	I-III	I-I	
	Climatic Category		40/125/21	40/125/21	
	Pollution Degree		2	2	
DIN V VDE V 0884-17 (1)(2)					
V _{IORM}	Maximum Repetitive Isolation Voltage	AC voltage	1700	700	V _{PK}
V _{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDb test	1200	500	V _{RMS}
		DC voltage	1700	700	V _{DC}
V _{IOTM}	Maximum Transient Isolation Voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production)	7000	5300	V _{PK}
V _{IOSM}	Maximum Surge Isolation Voltage ⁽³⁾	Test method per IEC 62368-1, 1.2/50 μs waveform, V _{TEST} = 1.3 × V _{IOSM} (qualification)	6500	5000	V _{PK}
q _{pd}	Apparent Charge	Method a, after input/output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤ 5	≤ 5	pC
		Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤ 5	≤ 5	
		Method b1; at routine test (100% production) and preconditioning (type	≤ 5	≤ 5	

±250-mV or ±50-mV Input Isolated Delta-Sigma Modulators

Parameter		Conditions	Value		Unit
			WSOP8	TSSOP8	
		test), $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini} = 1 \text{ s}$; $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m = 1 \text{ s}$			
C _{IO}	Isolation Capacitance	$V_{IO} = 0.4 \times \sin(2\pi ft)$, $f = 1 \text{ MHz}$	~0.5	~0.5	pF
R _{IO}	Isolation Resistance	$V_{IO} = 500 \text{ V}$, $T_A = 25^\circ\text{C}$	$> 10^{12}$	$> 10^{12}$	Ω
		$V_{IO} = 500 \text{ V}$, $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	$> 10^{11}$	$> 10^{11}$	Ω
		$V_{IO} = 500 \text{ V}$ at $T_S = 150^\circ\text{C}$	$> 10^9$	$> 10^9$	Ω
UL 1577					
V _{ISO}	Withstanding Isolation Voltage	$V_{TEST} = V_{ISO}$, $t = 60 \text{ s}$ (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1 \text{ s}$ (100% production)	5000	3750	V _{RMS}

- (1) All pins on each side of the barrier are tied together creating a two-terminal device.
- (2) This coupler is suitable for safe electrical insulation only within the safety operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing must be carried out in oil.

Safety-Related Certifications

VDE	UL	TUV	CQC	CSA	CB
Certified according to DIN VDE V 0884-17	Certified according to UL 1577 and CSA Component Acceptance Notice 5A	Certified according to EN IEC 62368-1 and EN IEC 61010-1	Certified according to GB 4943.1	Certified CSA C22.2 No. 62368-1 and CAN/CSA-C22.2 No. 60601-1	Certified according to EN IEC 62368-1
Certificate No. 40054570	Report Reference E524241	Registration No. AK506327310001	Certificate No. CQC23001393276	Certificate No. UL-CA-2336696-1	Ref. Certif. No. CN59992

Package Characteristics of TPA8101-DG5R and TPA8102-DG5R

Parameter		Test Conditions	Value	Unit
CLR	External Clearance	Shortest pin-to-pin distance through air	≥ 1	mm
CPG	External Creepage	Shortest pin-to-pin distance across the package surface	≥ 1	mm
CTI	Comparative Tracking Index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material Group	According to IEC 60664-1	I	
C _{IO}	Capacitance, input to output	V _{IO} = 0.5 V _{PP} at 1 MHz	~0.5	pF
R _{IO}	Resistance, input to output	T _A = 25°C	$> 10^{12}$	Ω

Safety Limiting Values

Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
Safety Input, Output or Supply Current	$R_{\theta JA} = 85^{\circ}\text{C/W}$, $VDD1 = VDD2 = 5.5\text{ V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$, WSOP8 package			267	mA
	$R_{\theta JA} = 191^{\circ}\text{C/W}$, $VDD1 = VDD2 = 5.5\text{ V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$, TSSOP8 package			119	mA
	$R_{\theta JA} = 39.5^{\circ}\text{C/W}$, $VDD1 = VDD2 = 5.5\text{ V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$, DFN2.7X3.5-8 package			575	mA
	$R_{\theta JA} = 85^{\circ}\text{C/W}$, $VDD1 = VDD2 = 3.6\text{ V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$, WSOP8 package			408	mA
	$R_{\theta JA} = 191^{\circ}\text{C/W}$, $VDD1 = VDD2 = 3.6\text{ V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$, TSSOP8 package			182	mA
	$R_{\theta JA} = 39.5^{\circ}\text{C/W}$, $VDD1 = VDD2 = 3.6\text{ V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$, DFN2.7X3.5-8 package			879	mA
Safety Total Power	$R_{\theta JA} = 85^{\circ}\text{C/W}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$, WSOP8 package			1470	mW
	$R_{\theta JA} = 191^{\circ}\text{C/W}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$, TSSOP8 package			655	mW
	$R_{\theta JA} = 39.5^{\circ}\text{C/W}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$, DFN2.7X3.5-8 package			3165	mW
Maximum Safety Temperature				150	$^{\circ}\text{C}$

(1) The assumed junction-to-air thermal resistance in the [Thermal Information](#) is that of a device installed on a high-K test board for leaded surface-mount packages.

±250-mV or ±50-mV Input Isolated Delta-Sigma Modulators
Electrical Characteristics—TPA8101

All test conditions: minimum and maximum specifications are at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 3.0\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $V_{INP} = -250\text{ mV}$ to $+250\text{ mV}$, and $V_{INN} = 0\text{ V}$; typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog Input						
V_{Clipping}	Differential Input Voltage before Clipping Output	$V_{INP} - V_{INN}$		±320		mV
V_{FSR}	Specified Linear Differential Full-Scale	$V_{INP} - V_{INN}$	−250		250	mV
V_{CM}	Specified Common-Mode Input Voltage	$(V_{INP} + V_{INN}) / 2$ to GND1	−0.16		$V_{DD1} - 2.5$	V
	Absolute Common-Mode Input Voltage ⁽¹⁾	$(V_{INN} + V_{INP}) / 2$ to GND1	−2		V_{DD1}	V
V_{CMov}	Common-Mode Overvoltage Detection Level		$V_{DD1} - 2.4$			V
CMRR	Common-Mode Rejection Ratio	$f_{\text{IN}} = 0\text{ Hz}$, $V_{\text{CM min}} \leq V_{\text{CM}} \leq V_{\text{CM max}}$		−95		dB
		$f_{\text{IN}} = 10\text{ kHz}$, $V_{\text{CM min}} \leq V_{\text{CM}} \leq V_{\text{CM max}}$		−100		
C_{IND}	Differential Input Capacitance			1		pF
R_{IN}	Single-Ended Input Resistance	$V_{INN} = \text{GND1}$		19		kΩ
R_{IND}	Differential Input Resistance			22		kΩ
I_{IB}	Input Bias Current	$V_{INP} = V_{INN} = \text{GND1}$, $I_{\text{IB}} = (I_{\text{IBP}} + I_{\text{IBN}}) / 2$	−22	−17		μA
TC_{IB}	Input Bias Current Drift			1		nA/°C
BW_{IN}	Input Bandwidth			1.2		MHz
DC Accuracy						
DNL	Differential Nonlinearity ⁽¹⁾	Resolution: 16 bits	−0.99		0.99	LSB
INL	Integral Nonlinearity ⁽¹⁾	Resolution: 16 bits	−4	±1	4	LSB
E_{O}	Offset Error	$V_{DD1} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$, $V_{INP} = V_{INN} = \text{GND1}$	−150	±5	150	μV
TCE_{O}	Offset Error Thermal Drift ⁽¹⁾		−1	±0.15	1	μV/°C
E_{G}	Gain Error	at 25°C	−0.3	±0.005	0.3	%
TCE_{G}	Gain Error Thermal Drift ⁽¹⁾		−40	±20	40	ppm/°C
PSRR	Power-Supply Rejection Ratio	$V_{INP} = V_{INN} = \text{GND1}$, $3.0\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, at DC		90		dB
		$V_{INP} = V_{INN} = \text{GND1}$, $V_{DD1} = 5\text{ V}$, 10 kHz, 100-mV ripple		80		dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AC Accuracy						
SNR	Signal-to-Noise Ratio	f _{IN} = 1 kHz		86		dB
SINAD	Signal-to-Noise + Distortion	f _{IN} = 1 kHz		85		dB
THD	Total Harmonic Distortion	VDD1 = 5.0 V, 5 MHz ≤ f _{CLKIN} ≤ 20 MHz, f _{IN} = 1 kHz		−82		dB
		VDD1 = 3.3 V, 5 MHz ≤ f _{CLKIN} ≤ 20 MHz, f _{IN} = 1 kHz		−80		dB
SFDR	Spurious-Free Dynamic Range	f _{IN} = 1 kHz		84		dB
Digital Inputs/Outputs						
I _{IN}	Input Current ⁽¹⁾	GND2 ≤ V _{IN} ≤ VDD2			7	μA
C _{IN}	Input Capacitance			4		pF
V _{IH}	High-Level Input Voltage ⁽¹⁾		0.7 × VDD2			V
V _{IL}	Low-Level Input Voltage ⁽¹⁾				0.3 × VDD2	V
C _{LOAD}	Output Load Capacitance	f _{CLKIN} = 20 MHz		30		pF
V _{OH}	High-Level Output Voltage	I _{OH} = −20 μA	VDD2 − 0.1			V
		I _{OH} = −4 mA	VDD2 − 0.4			V
V _{OL}	Low-Level Output Voltage	I _{OL} = 20 μA			0.1	V
		I _{OL} = 4 mA			0.4	V
Power Supply						
VDD1 _{UV}	Undervoltage Detection Threshold Voltage of VDD1	VDD1 falling		2.1	2.4	V
I _{DD1}	High-Side Supply Current	3.0 V ≤ VDD1 ≤ 5.5 V		13	18	mA
I _{DD2}	Low-Side Supply Current	3.0 V ≤ VDD2 ≤ 5.5V		4	8	mA
Switching Characteristics ⁽¹⁾						
f _{CLKIN}	CLKIN Clock Frequency	4.5 V ≤ VDD2 ≤ 5.5 V	5		21	MHz
		3.0 V ≤ VDD2 ≤ 5.5 V	5		20	
t _{CLKIN}	CLKIN Clock Period	4.5 V ≤ VDD2 ≤ 5.5 V	47.6		200	ns
		3.0 V ≤ VDD2 ≤ 5.5 V	50		200	
t _{HIGH}	CLKIN Clock High Time		20	25	120	ns
t _{LOW}	CLKIN Clock Low Time		20	25	120	ns
t _H	DOUT Hold Time after Rising Edge of CLKIN	C _{LOAD} = 15 pF	3.1			ns
t _D	Rising Edge of CLKIN to DOUT Valid Delay	C _{LOAD} = 15 pF			15	ns

$\pm 250\text{-mV}$ or $\pm 50\text{-mV}$ Input Isolated Delta-Sigma Modulators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	DOUT Rise Time	10% to 90%, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, $C_{LOAD} = 15\text{ pF}$		0.8	3	ns
		10% to 90%, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, $C_{LOAD} = 15\text{ pF}$		0.8	3	
t_f	DOUT Fall Time	90% to 10%, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, $C_{LOAD} = 15\text{ pF}$		0.8	3	ns
		90% to 10%, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, $C_{LOAD} = 15\text{ pF}$		0.8	3	
t_{START}	Interface Startup Time	V_{DD2} at 3 V (min) to DOUT valid with $V_{DD1} \geq 3\text{ V}$		32		CLKIN Cycles
t_{ASTART}	Analog Startup Time	V_{DD1} step to 3.0 V with $V_{DD2} \geq 3\text{ V}$, 0.1% settling		0.5		ms

(1) Provided by bench tests or design simulation.

Electrical Characteristics—TPA8102

Minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 3.0\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $V_{INP} = -50\text{ mV}$ to $+50\text{ mV}$, and $V_{INN} = 0\text{ V}$; typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Analog Input						
V _{Clipping}	Differential input voltage before clipping output	V _{INP} – V _{INN}		±64		mV
V _{FSR}	Specified linear differential full-scale	V _{INP} – V _{INN}	–50		50	mV
V _{CM}	Specified common-mode input voltage	(V _{INP} + V _{INN}) / 2 to GND1	–0.032		V _{DD1} – 2.5	V
	Absolute common-mode input voltage ⁽¹⁾	(V _{INN} + V _{INP}) / 2 to GND1	–2		V _{DD1}	V
V _{CMov}	Common-mode overvoltage detection level		V _{DD1} – 2.4			V
CMRR	Common-mode rejection ratio	f _{IN} = 0 Hz, V _{CM} min ≤ V _{CM} ≤ V _{CM} max		–98		dB
		f _{IN} = 10 kHz, V _{CM} min ≤ V _{CM} ≤ V _{CM} max		–98		
C _{IND}	Differential input capacitance			1		pF
R _{IN}	Single-ended input resistance	V _{INN} = GND1		4.75		kΩ
R _{IND}	Differential input resistance			4.9		kΩ
I _{IB}	Input bias current	V _{INP} = V _{INN} = GND1, I _{IB} = (I _{IBP} + I _{IBN}) / 2	–22	–17		μA
TCI _{IB}	Input bias current drift			1		nA/°C
BW _{IN}	Input bandwidth			1.2		MHz
DC Accuracy						
DNL	Differential nonlinearity ⁽¹⁾	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity ⁽¹⁾	Resolution: 16 bits	–4	±1	4	LSB
E _O	Offset error	V _{DD1} = 5 V, T _A = 25°C, V _{INP} = V _{INN} = GND1	–50	±2.5	50	μV
TCE _O	Offset error thermal drift ⁽¹⁾		–1	±0.25	1	μV/°C
E _G	Gain error	at 25°C	–0.3	±0.01	0.3	%
TCE _G	Gain error thermal drift ⁽¹⁾		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	V _{INP} = V _{INN} = GND1, 3.0 V ≤ V _{DD1} ≤ 5.5 V, at dc		108		dB
		V _{INP} = V _{INN} = GND1, V _{DD1} = 5 V, 10 kHz, 100-mV ripple		90		dB
AC Accuracy						

±250-mV or ±50-mV Input Isolated Delta-Sigma Modulators

Parameter		Conditions	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	f _{IN} = 1 kHz		82.5		dB
SINAD	Signal-to-noise + distortion	f _{IN} = 1 kHz		82.3		dB
THD	Total harmonic distortion	VDD1 = 5.0 V, 5 MHz ≤ f _{CLKIN} ≤ 20 MHz, f _{IN} = 1 kHz		−98		dB
		VDD1 = 3.3 V, 5 MHz ≤ f _{CLKIN} ≤ 20 MHz, f _{IN} = 1 kHz		−93		dB
SFDR	Spurious-free dynamic range	f _{IN} = 1 kHz		100		dB
Digital Inputs/Outputs						
I _{IN}	Input current ⁽¹⁾	GND2 ≤ V _{IN} ≤ VDD2			7	μA
C _{IN}	Input capacitance			4		pF
V _{IH}	High-level input voltage ⁽¹⁾		0.7 × VDD2			V
V _{IL}	Low-level input voltage ⁽¹⁾				0.3 × VDD2	V
CLOAD	Output load capacitance	f _{CLKIN} = 20 MHz		30		pF
VOH	High-level output voltage	I _{OH} = −20 μA	VDD2 − 0.1			V
		I _{OH} = −4 mA	VDD2 − 0.4			V
VOL	Low-level output voltage	I _{OL} = 20 μA			0.1	V
		I _{OL} = 4 mA			0.4	V
Power Supply						
VDD1 _{UV}	undervoltage detection threshold voltage of VDD1	VDD1 falling		2.1	2.4	V
I _{DD1}	High-side supply current	3.0 V ≤ VDD1 ≤ 5.5 V		13	18	mA
I _{DD2}	Low-side supply current	3.0 V ≤ VDD2 ≤ 5.5V		4	8	mA
Switching Characteristics ⁽¹⁾						
f _{CLKIN}	CLKIN clock frequency	4.5 V ≤ VDD2 ≤ 5.5 V	5		21	MHz
		3.0 V ≤ VDD2 ≤ 5.5 V	5		20	
t _{CLKIN}	CLKIN clock period	4.5 V ≤ VDD2 ≤ 5.5 V	47.6		200	ns
		3.0 V ≤ VDD2 ≤ 5.5 V	50		200	
t _{HIGH}	CLKIN clock high time		20	25	120	ns
t _{LOW}	CLKIN clock low time		20	25	120	ns
t _H	DOUT hold time after rising edge of CLKIN	C _{LOAD} = 15 pF	3.1			ns
t _D	Rising edge of CLKIN to DOUT valid delay	C _{LOAD} = 15 pF			15	ns

Parameter	Conditions	Min	Typ	Max	Unit
t_r	10% to 90%, $2.7\text{ V} \leq \text{VDD2} \leq 3.6\text{ V}$, $C_{\text{LOAD}} = 15\text{ pF}$		0.8	3	ns
	10% to 90%, $4.5\text{ V} \leq \text{VDD2} \leq 5.5\text{ V}$, $C_{\text{LOAD}} = 15\text{ pF}$		0.8	3	
t_f	90% to 10%, $2.7\text{ V} \leq \text{VDD2} \leq 3.6\text{ V}$, $C_{\text{LOAD}} = 15\text{ pF}$		0.8	3	ns
	90% to 10%, $4.5\text{ V} \leq \text{VDD2} \leq 5.5\text{ V}$, $C_{\text{LOAD}} = 15\text{ pF}$		0.8	3	
t_{START}	Interface startup time		32		CLKIN cycles
t_{ASTART}	Analog startup time		0.5		ms

(1) Provided by bench test or design simulation.

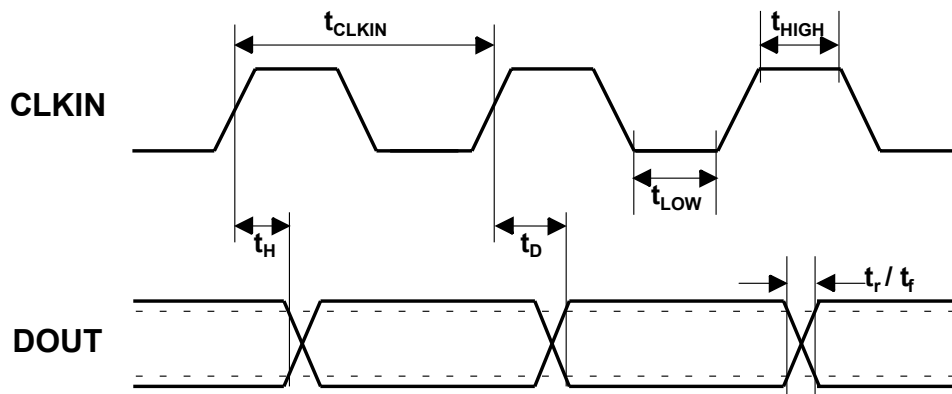


Figure 1. Digital Interface Timing of TPA8101 and TPA8102

Typical Performance Characteristics

All test conditions: $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -250\text{ mV}$ to 250 mV for TPA8101, $V_{INP} = -50\text{ mV}$ to 50 mV for TPA8102, $V_{INN} = 0\text{ V}$, $f_{CLKIN} = 20\text{ MHz}$, and sinc^3 filter with $\text{OSR} = 256$, unless otherwise noted.

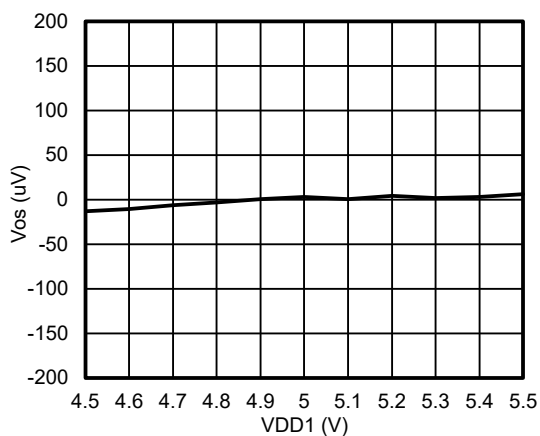


Figure 2. V_{os} vs. V_{DD1}

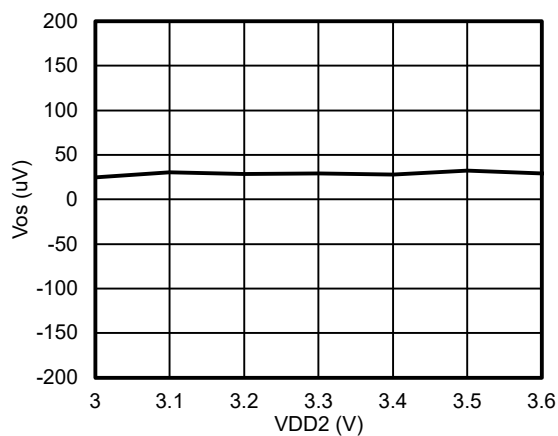


Figure 3. V_{os} vs. V_{DD2}

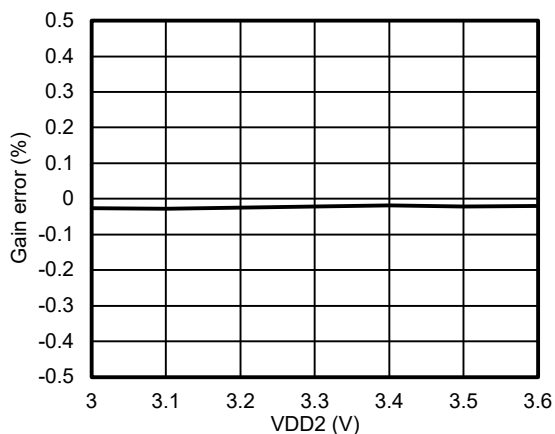


Figure 4. Gain Error vs. V_{DD2}

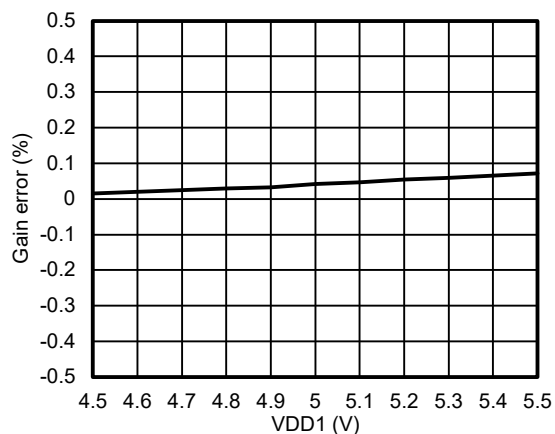
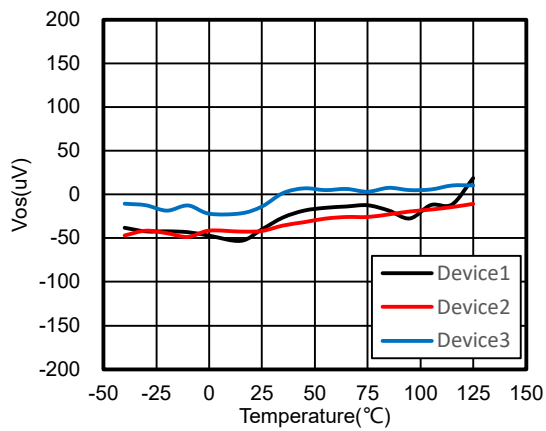
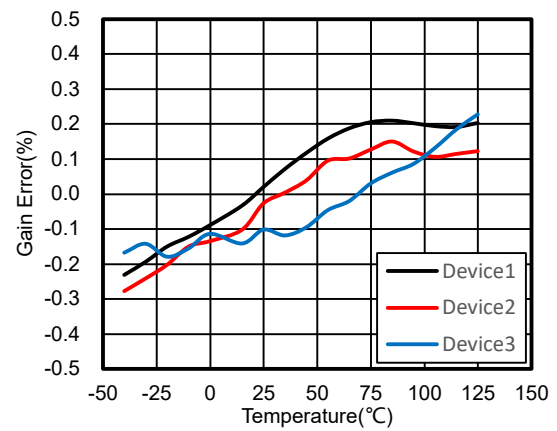
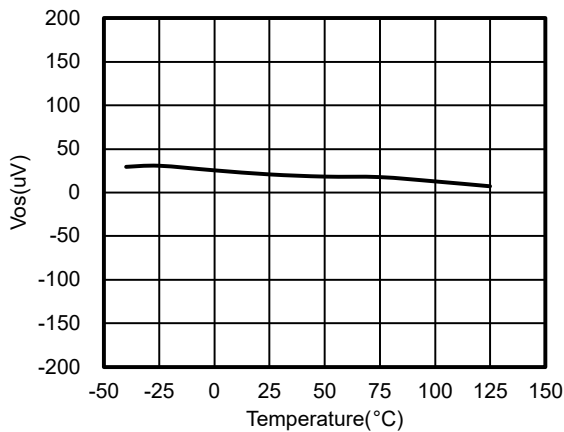
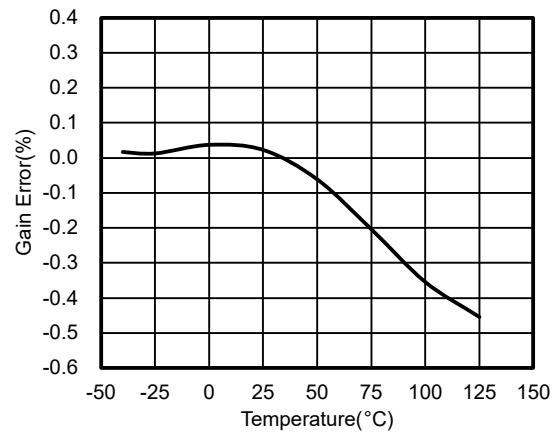
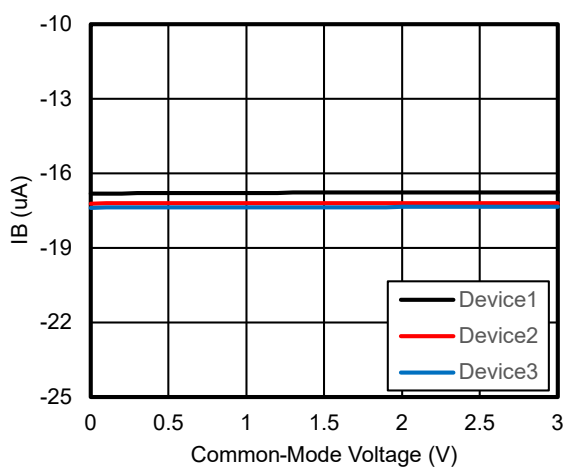
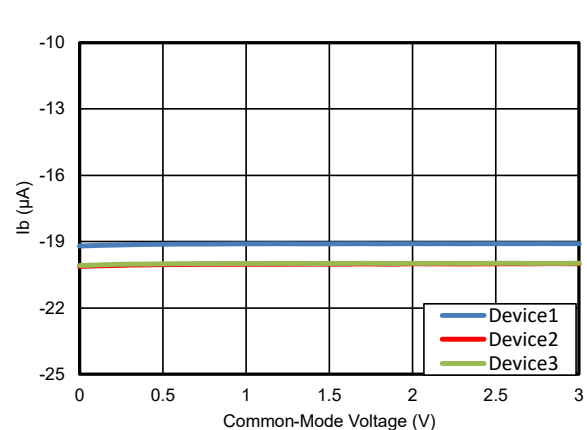
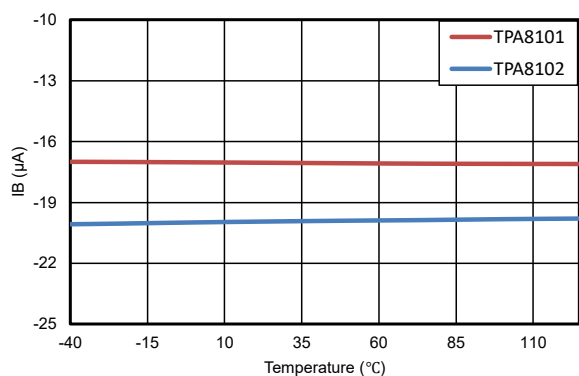
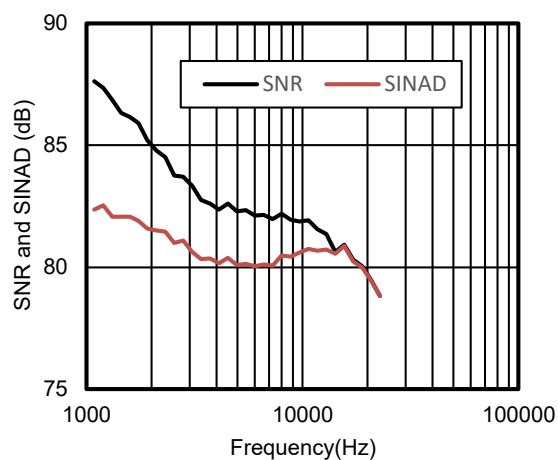
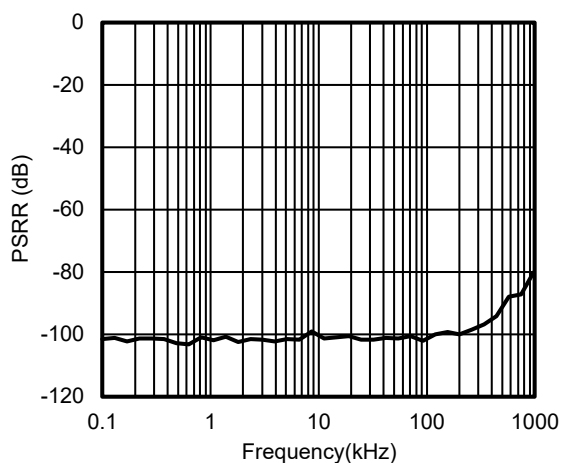
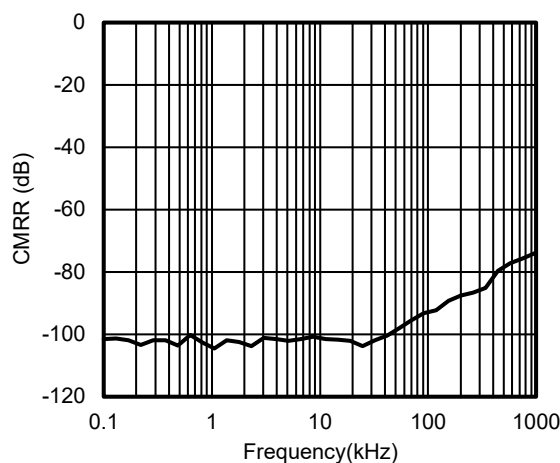
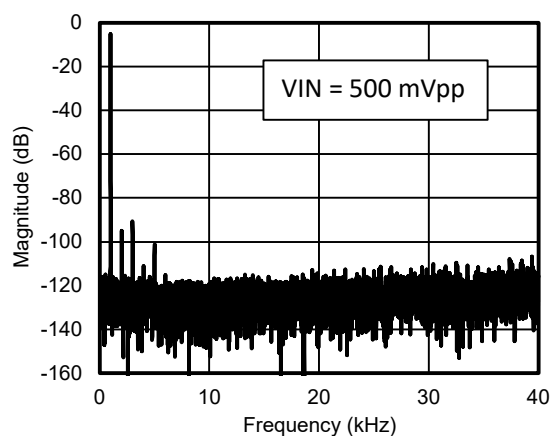
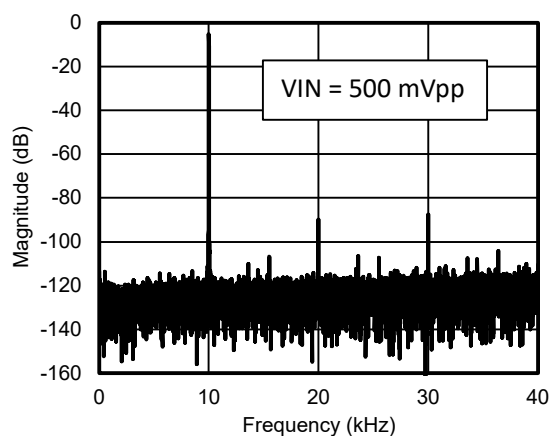


Figure 5. Gain Error vs. V_{DD1}


Figure 6. V_{os} vs. Temperature of TPA8101

Figure 7. Gain Error vs. Temperature of TPA8101

Figure 8. V_{os} vs. Temperature of TPA8102

Figure 9. Gain Error vs. Temperature of TPA8102

Figure 10. I_b vs. Common-Mode Voltage of TPA8101

Figure 11. I_b vs. Common-Mode Voltage of TPA8102


Figure 12. I_B vs. Temperature

Figure 13. SNR and SINAD vs. Input Signal Frequency of TPA8101

Figure 14. VDD1 PSRR vs. Frequency of TPA8101

Figure 15. CMRR vs. Frequency of TPA8101

Figure 16. TPA8101 Frequency Spectrum with 1-kHz Input Signal

Figure 17. TPA8101 Frequency Spectrum with 10-kHz Input Signal

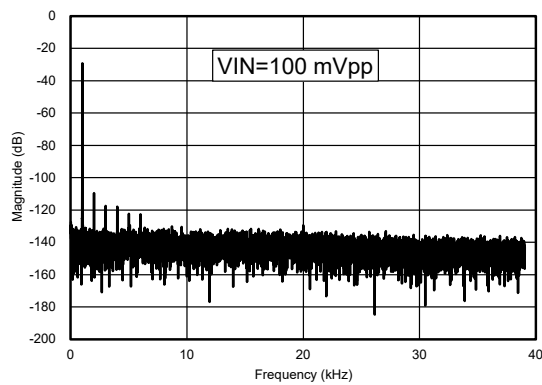


Figure 18. TPA8102 Frequency Spectrum with 1-kHz Input Signal

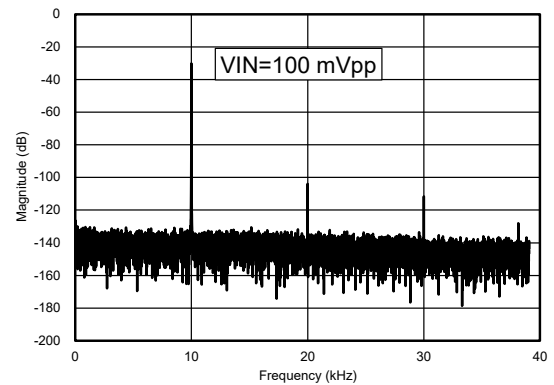


Figure 19. TPA8102 Frequency Spectrum with 10-kHz Input Signal

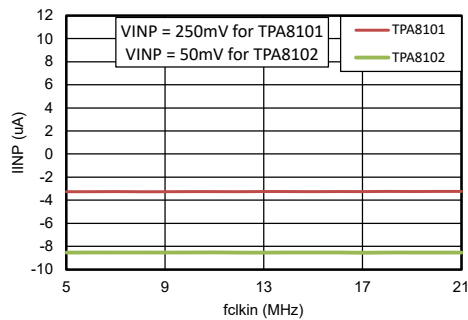


Figure 20. Input Current vs. Clock Frequency

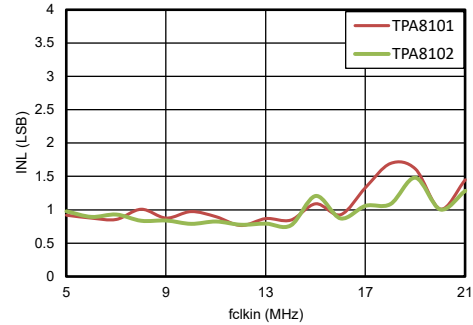


Figure 21. Integral Nonlinearity vs. Clock Frequency

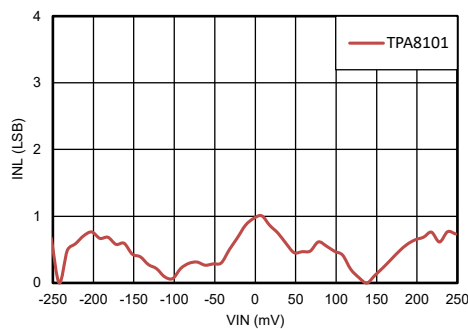


Figure 22. TPA8101 Integral Nonlinearity vs. Input Voltage

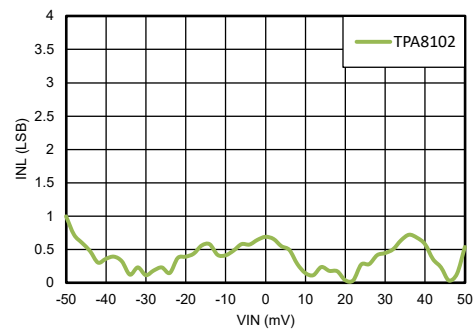


Figure 23. TPA8102 Integral Nonlinearity vs. Input Voltage

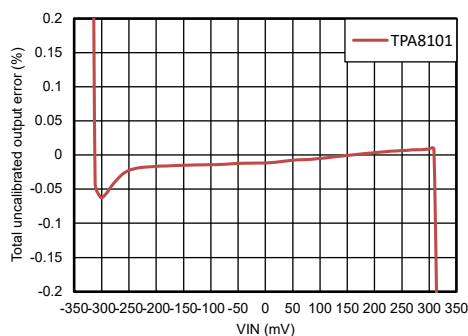
± 250 -mV or ± 50 -mV Input Isolated Delta-Sigma Modulators


Figure 24. TPA8101 Total Uncalibrated Output Error vs. Input Voltage

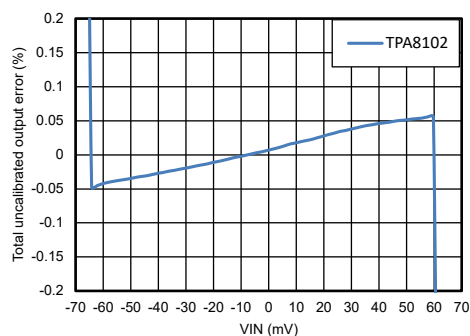


Figure 25. TPA8102 Total Uncalibrated Output Error vs. Input Voltage

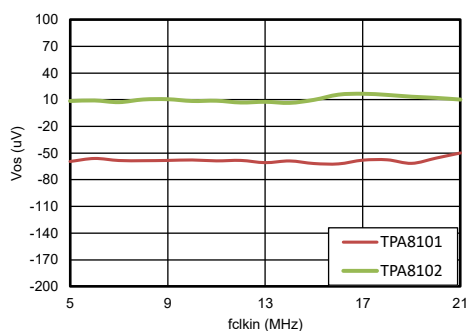


Figure 26. Vos vs. Clock Frequency

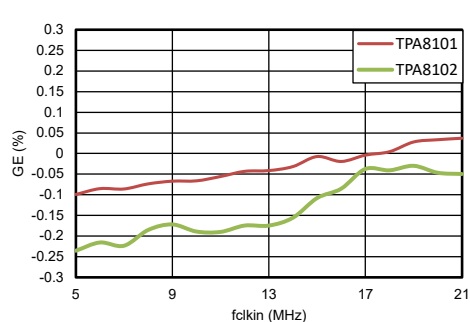


Figure 27. Gain Error vs. Clock Frequency

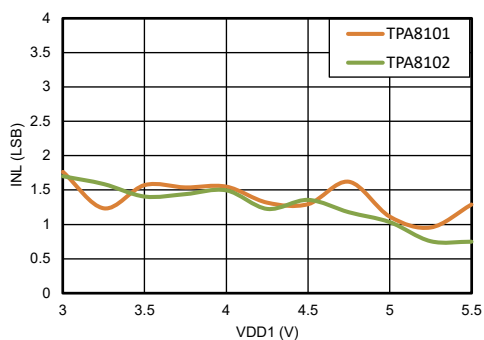


Figure 28. Integral Nonlinearity vs. High-Side Supply Voltage

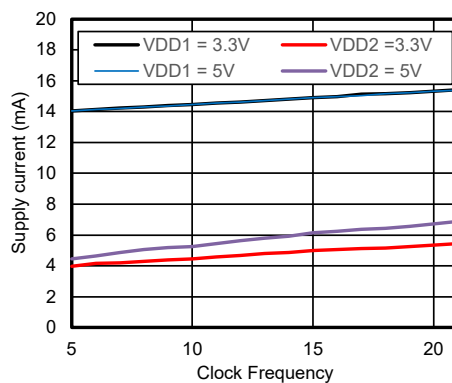


Figure 29. Supply Current vs. Clock Frequency

Detailed Description

Overview

The differential analog input of the device is a fully-differential amplifier feeding the switched-capacitor input of a delta-sigma ($\Delta\Sigma$) modulator stage which digitizes the input signal into a 1-bit output stream. The isolated data output DOUT of the converter provides a stream of digital zeros and ones that are synchronous to the clock source at the CLKIN pin with a frequency in the range of 5 MHz to 21 MHz. The time average of this serial bitstream output is proportional to the analog input voltage.

Based on the SiO_2 -based and double-capacitive isolation barrier, the digital modulation and isolation barrier characteristics provide high reliability and common-mode transient immunity for the device.

Functional Block Diagram

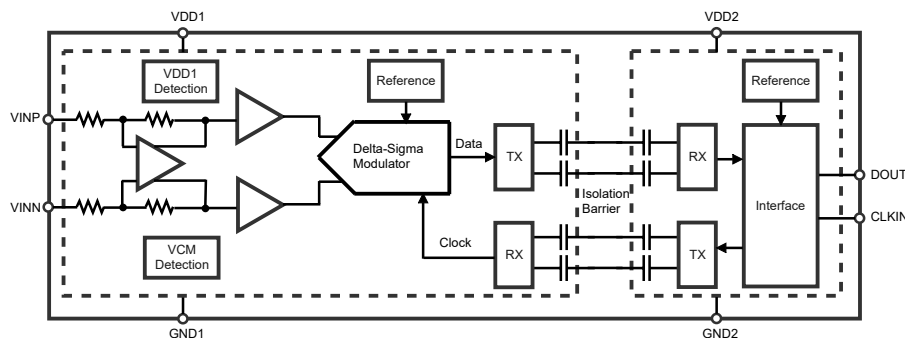


Figure 30. Functional Block Diagram

Feature Description

Fail-Safe Output

The device provides a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active in two cases:

- When the VDD1 is missing, or the voltage at VDD1 is lower than $VDD1_{UV}$ (the undervoltage detection threshold voltage of VDD1), the output DOUT of the device provides a steady-state bitstream of logic 0's.
- When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN}) / 2$, exceeds the V_{CMov} (the minimum common-mode overvoltage detection level), the output DOUT of the device provides a steady-state bitstream of logic 1's.

Output Behavior in Case of a Full-Scale Input

To distinguish from the output, if a full-scale input signal is applied to the device, the device generates a single one or zero every 128 bits at DOUT, depending on the polarity of the input signal.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 31 shows the typical application schematic.

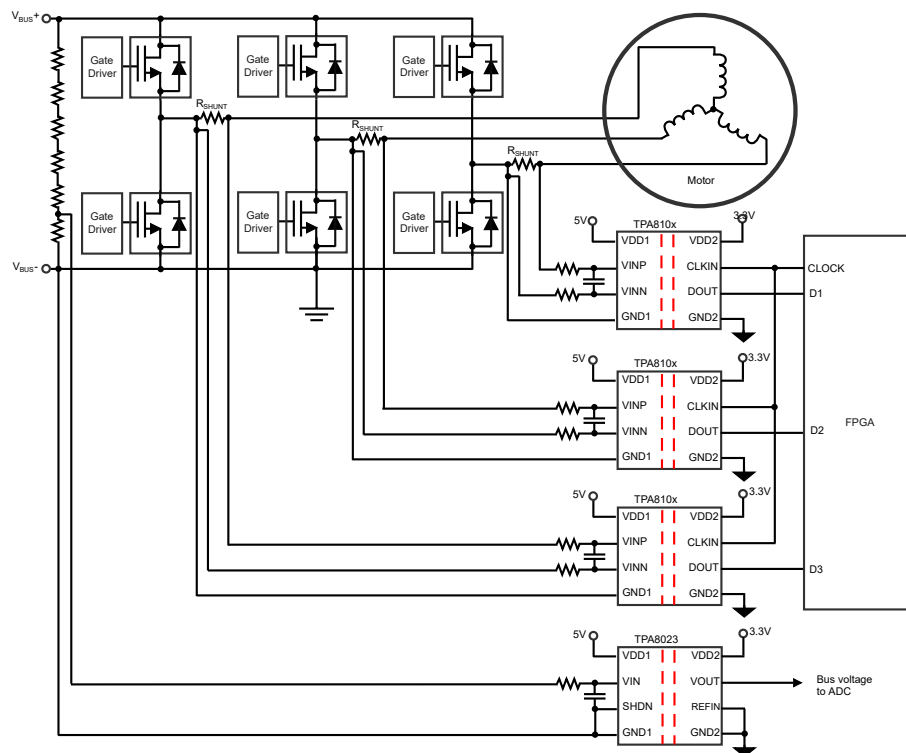


Figure 31. Application Schematic

Motor Drive Application

Isolated amplifiers are widely used in frequency inverters, which are critical parts of industrial motor drives, servo control systems, and other industrial applications.

The TPA810x is optimized for current sensing applications with shunt resistors. Figure 31 shows a typical operation of the device for current sensing in a motor drive application. Phase current is measured by the shunt resistors, R_{SHUNT} . The differential input and the high common-mode transient immunity of the device ensure reliable and accurate operation in high-noise environments.

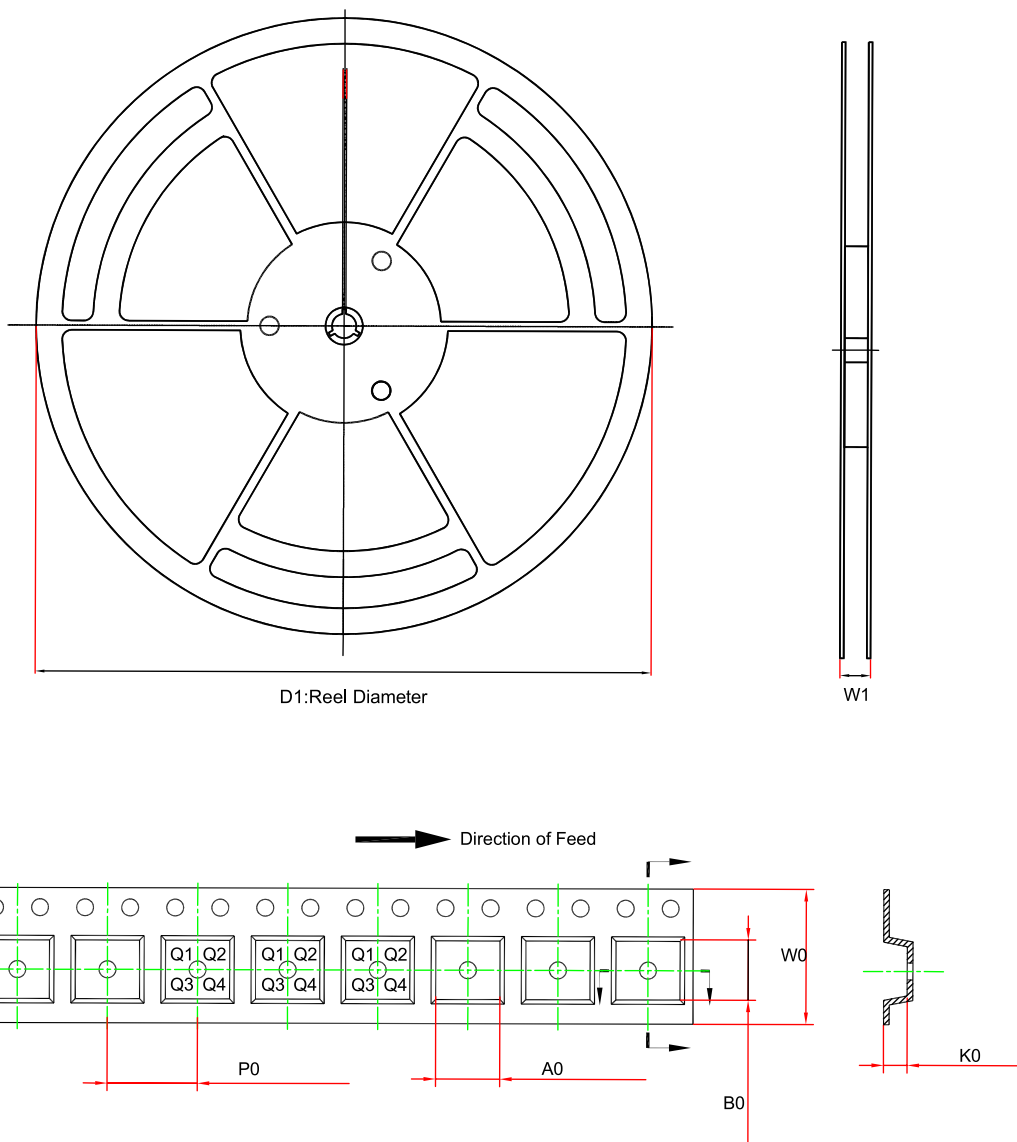
The DC bus voltage is measured by the TPA8023 with a high-impedance input and a wide input voltage range.

 ± 250 -mV or ± 50 -mV Input Isolated Delta-Sigma Modulators**Power Supply Recommendation**

In a typical frequency inverter application, the high-side power supply (VDD1) of the device is derived from the floating power supply of the upper gate driver. A Zener diode with a shunt resistor can be used to provide high-side power supply of the device, or a low-cost low-dropout regulator (LDO) may be used to reduce the noise on the power supply. Place a 0.1- μ F bypass capacitor as close as possible to the VDD1 pin of the device for best performance, and an additional 1- μ F to 10- μ F capacitor may be used for better filtering.

To decouple the low-side power supply, place a 0.1- μ F capacitor to the VDD2 pin of the device as close as possible, and an additional 1- μ F to 10- μ F capacitor may be used for better filtering.

Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA8101-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16.0	16.0	Q1
TPA8101-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16.0	16.0	Q1
TPA8101-TS1R	TSSOP8	330	17.6	6.8	3.4	1.8	8.0	12.0	Q1
TPA8101-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12.0	16.0	Q1
TPA8101-DG5R	DFN2.7X3.5-8	330	17.6	3	3.8	1.1	8.0	12.0	Q2
TPA8102-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16.0	16.0	Q1
TPA8102-DG5R	DFN2.7X3.5-8	330	17.6	3	3.8	1.1	8.0	12.0	Q2

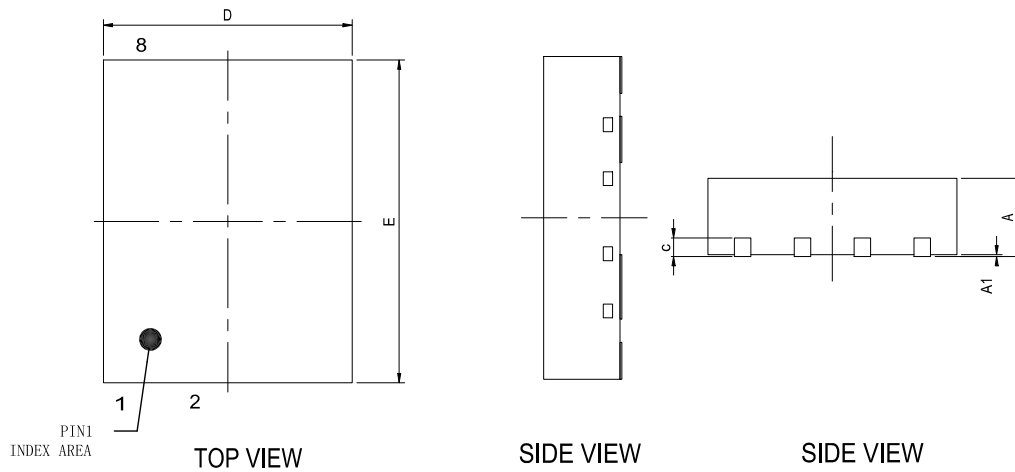
(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

DFN2.7X3.5-8

Package Outline Dimensions

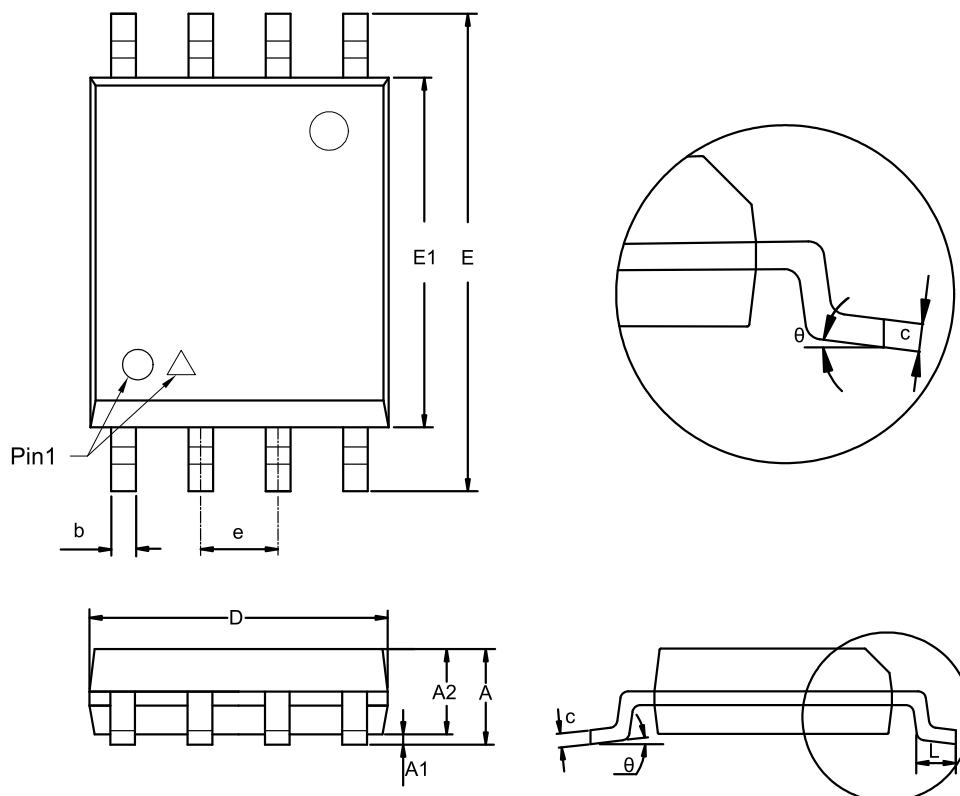
DG5(DFN2.7X3.5-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
c	0.203REF		0.008REF	
D	2.600	2.800	0.1024	0.1339
E	3.400	3.600	0.134	0.142
e	0.650BSC		0.026BSC	
e1	0.850BSC		0.033BSC	
e2	0.750BSC		0.030BSC	
D2	2.130	2.330	0.084	0.092
E2	0.400	0.600	0.016	0.024
E3	0.600	0.800	0.024	0.031
L	0.300	0.500	0.012	0.020

NOTES

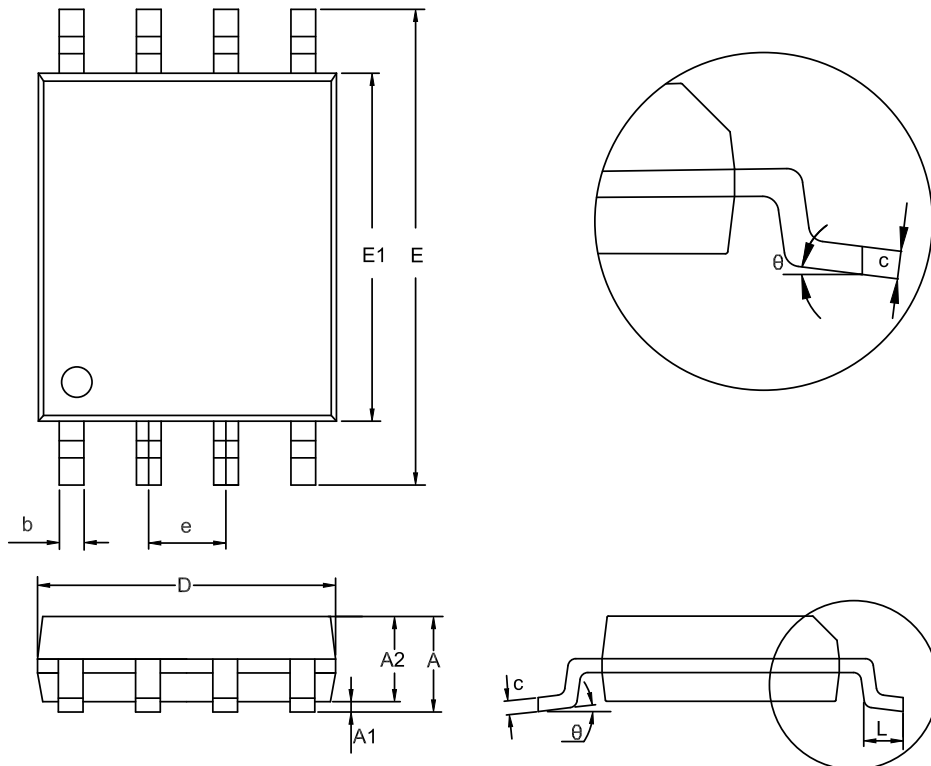
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

WSOP8
Package Outline Dimensions
SOA(WSOP-8-B)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
b	0.310	0.510	0.012	0.020
c	0.150	0.300	0.006	0.012
D	5.750	5.950	0.226	0.234
E	11.250	11.750	0.443	0.463
E1	7.400	7.600	0.291	0.299
e	1.270 BSC		0.050 BSC	
L	0.500	1.000	0.020	0.039
θ	0	8°	0	8°

NOTES

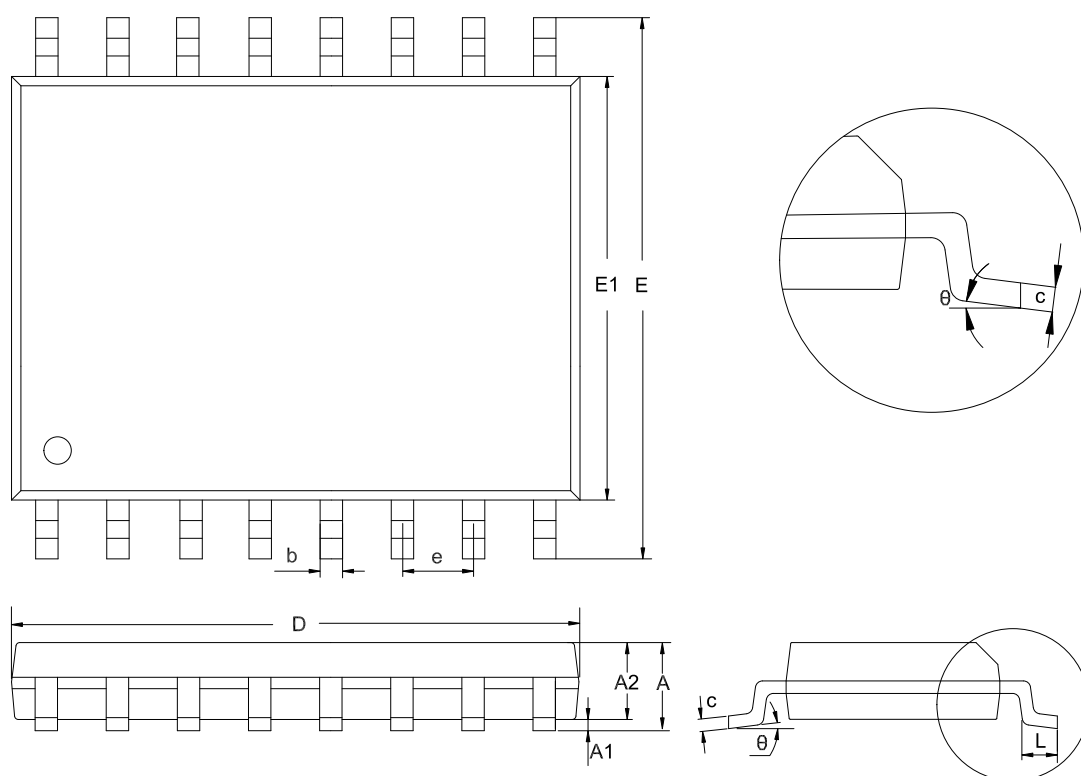
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TSSOP8
Package Outline Dimensions
TS1(TSSOP-8-A)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

WSOP16
Package Outline Dimensions
SOB(WSOP-16-A)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
b	0.350	0.450	0.014	0.018
c	0.200	0.290	0.008	0.011
D	10.100	10.500	0.398	0.413
E	10.100	10.600	0.398	0.417
E1	7.300	7.700	0.287	0.303
e	1.270 BSC		0.050 BSC	
L	0.500	0.850	0.020	0.033
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA8101-SOAR	-40 to 125°C	WSOP8	A8101	3	Tape and Reel, 1000	Green
TPA8101-SOAR-S ⁽¹⁾ ⁽²⁾	-40 to 125°C	WSOP8	A8101	3	Tape and Reel, 1000	Green
TPA8101-TS1R	-40 to 125°C	TSSOP8	A8101	3	Tape and Reel, 3000	Green
TPA8101-SOBR	-40 to 125°C	WSOP16	A8101	3	Tape and Reel, 1500	Green
TPA8101-DG5R	-40 to 125°C	DFN2.7X3.5-8	ACp	3	Tape and Reel, 5000	Green
TPA8102-SOAR	-40 to 125°C	WSOP8	A8102	3	Tape and Reel, 1000	Green
TPA8102-DG5R	-40 to 125°C	DFN2.7X3.5-8	ACx	3	Tape and Reel, 5000	Green

(1) Passed AEC-Q100 Reliability Test.

(2) For future products, contact the 3PEAK factory for more information and samples.

Green: Defines "Green" to mean RoHS compatible and free of halogen substances.

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