Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML22620

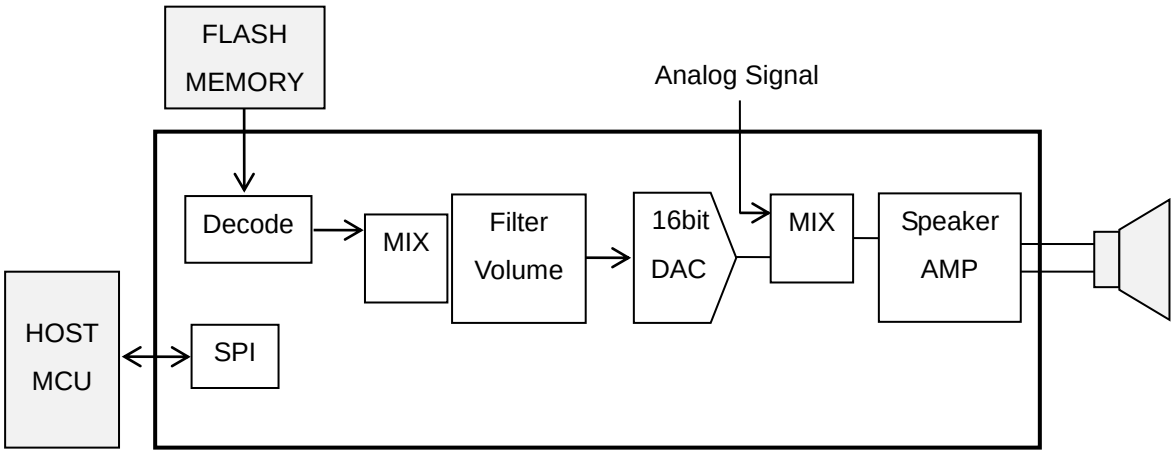
4-Channel Mixing Speech Synthesis LSI

■ Overview

ML22620 is a 4-channel mixing speech synthesis LSI with a serial flash memory interface for sound data. It is equipped with a clock synchronous serial interface.
It adopts a HQ-ADPCM*1, 16-bit D/A converter, and low-pass filter for high sound quality, and incorporates a 1.0W mono speaker amplifier for driving speakers directly. It is also equipped with a function to detect failure.
The functions necessary for sound output are integrated into a single chip, so that sound functions can be realized simply by adding this LSI.

● Memory capacity and maximum sound production time (HQ-ADPCM*1 algorithm, registered phrase 1024)

Product Name	Flash memory capacity	Maximum sound production time (sec)		
		f_S=8.0kHz	f_S =16.0kHz	f_S =32.0kHz
ML22620	128Mbits (Serial Flash Memory)	5240	2620	1310



Application Circuit

*1 HQ-ADPCM is "Ky's" high-quality audio compression technique.
"Ky's" is a registered trademark of Kyushu Institute of Technology, a national university corporation.

■ Feature

- Sound data
  - Speech synthesis algorithm: The algorithm can be specified for each phrase.
    HQ-ADPCM/4bit ADPCM2/8bit non-linear PCM /
    8bit Straight PCM/16bit Straight PCM
  - Sampling frequency: The sampling frequency can be specified for each phrase.
    10.7/21.3kHz,
    6.4/12.8/25.6kHz,
    8.0/16.0/32.0kHz,
    11.025/22.05/44.1kHz,
    12.0/24.0/48.0kHz
  - Maximum number of phrases: 4096 Phrases
- Edit ROM function
- Playback function
  - Repeat function: LOOP command
  - Mixing-function: Up to 4-channel
  - Volume adjustment function: CVOL command 128 levels (including off-state)
    AVOL command 16 levels (including off-state)
- Low-pass filter
- 16-bit D/A converter
- Speaker amplifier: Class AB/D 1. 0W 8Ω (SPV_{DD} =5V, Ta=25 ^{O}C)
- Line amplifier output: 10kΩ driving (Exclusive operation from speaker amplifier output)
- External analog sound input (at the time Class AB speaker amplifier choice, with analog mixing function)
- MCU command interface: Clock Synchronous Serial Interface
- Failure detection function
  - Speaker short detection: Speaker pin ground fault detection, speaker pin short detection
  - Speaker disconnection detection
  - Thermal detection
  - Clock error detection
  - Flash memory error detection
- Clock backup function
- Master clock frequency: 4.096MHz, 4.000MHz
- Power-supply voltage 2.7V to 5.5V
  DV_{DD}, SPV_{DD} and IOV_{DD} can be set independently. ($SPV_{DD} \geq DV_{DD}$)
- Operating temperature range: -40 ^{O}C to +85 ^{O}C *1

*1 The operating time of the speaker amplifier may be limited depending on the average ambient temperature (Ta) used.

■ Applications

● Consumer and Industrial equipment (e.g., Household appliances, Housing equipment, Office equipment, Measurement instrumentation, etc.).

【NOTE】

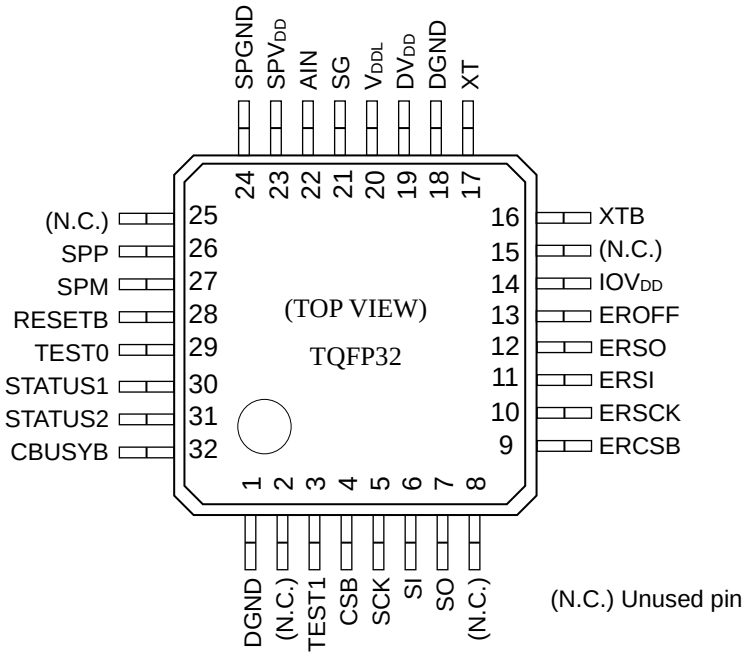
This product cannot be applicable for automotive use, automatic train control systems, and railway safety systems. Please contact ROHM sales office in advance if contemplating the integration of this product into applications that requires high reliability, such as transportation equipment for ships and railways, communication equipment for trunk lines, traffic signal equip.

■ Table format

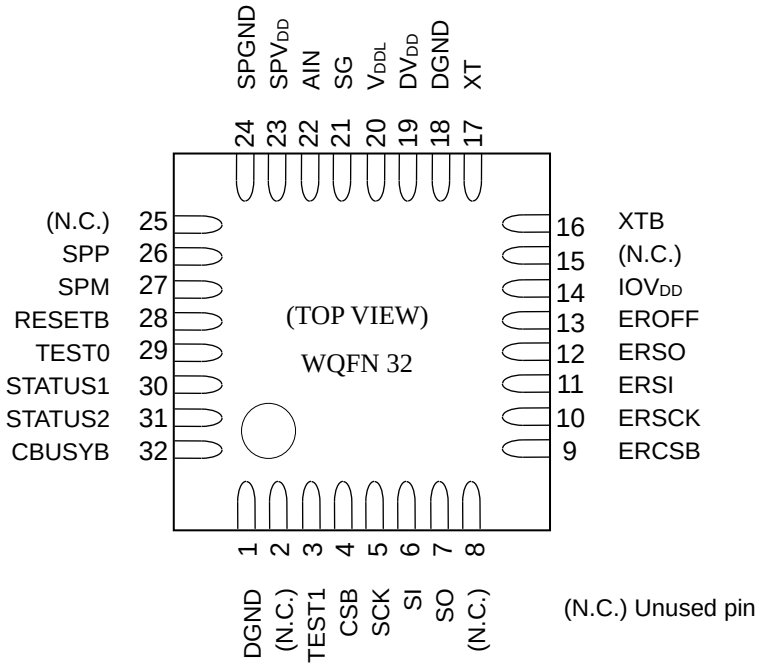
Package	Body size (including lead) [mm × mm]	Pin pitch [mm]	Packing form and Product name	
			Tray	Tape & Reel
32 pin plastic TQFP	7.0 × 7.0 (9.0 × 9.0)	0.80	ML22620TBZ0AX	ML22620TBZ0BX
32 pin plastic WQFN	5.0 × 5.0 (−)	0.50	ML22620GDZ05AX	ML22620GDZ05BX

■ Pin Configuration (TOP VIEW)

● ML22620TB



- ML22620GD


SPGND 24
SPVDD 23
AIN 22
SG 21
VDDL 20
DVDD 19
DGND 18
XT 17
(N.C.) 25
SPP 26
SPM 27
RESETB 28
TEST0 29
STATUS1 30
STATUS2 31
CBUSYB 32
16 XTB
15 (N.C.)
14 IOVDD
13 EROFF
12 ERSO
11 ERSI
10 ERSCK
9 ERCSB
(TOP VIEW)
WQFN 32
1 DGND
2 (N.C.)
3 TEST1
4 CSB
5 SCK
6 SI
7 SO
8 (N.C.)
(N.C.) Unused pin

■ Pin Description

Pin	Symbol	I/O	Attribute	Description	Initial value *1
1,18	DGND	G	-	Digital ground pin.	—
3	TEST1	O	-	Output pin for testing. Leave open.	Hi-Z
4	CSB	I	Negative	Synchronous serial interface chip select pin. The SCK and SI inputs are accepted only when this pin is at the "L" level.	H
5	SCK	I	-	Synchronous serial interface clock input pin.	L
6	SI	I	-	Synchronous serial interface data input pin. Data is fetched in synchronization with SCK.	L
7	SO	O	-	Synchronous serial interface data output pin. When the CSB pin is at an "L" level, data is output in synchronization with SCK. When the CSB pin is at an "H" level, this pin enters a high-impedance state.	Hi-Z
9	ERCSB	O	Negative	Serial flash memory interface chip select output pin. Output the "H" level during non-access and the "L" level during access. Setting the EROFF pin to "L" enables output.	H*2
10	ERSCK	O	-	Serial flash memory interface serial clock output pin. Setting the EROFF pin to "L" enables output.	L*2
11	ERSI	I	-	Serial flash memory interface serial data input pin. Setting the EROFF pin to "L" enables input. A pull-down resistor is internally connected.	L
12	ERSO	O	-	Serial flash memory interface serial data output pin. Setting the EROFF pin to "L" enables output.	L*2
13	EROFF	I	Positive	Pin to disable the serial flash memory interface. When this bit is set to "L", the serial flash memory interface pin is enabled. A pull-down resistor is internally connected. Set this pin to "L" during playback operation using serial flash memory. When this pin set to "H", the serial flash memory interface is in a condition of high-impedance. Set this bit to "H" for onboard rewriting.	L

*1 Initial value at reset input and power-down. The pin whose IO is "I" indicates a fixed level from outside.
*2 If an error in the Flash memory is detected, intitial value will be output.

Pin	Symbol	I/O	Attribute	Description	Initial value *1
14	IOV_{DD}	P	-	Serial flash memory interface power supply pin. Connect a bypass capacitor between this pin and the DGND pin.	—
16	XTB	O	Negative	Crystal or ceramic resonator connection pin. When an external clock is used, leave it open and capacitor is not required when a crystal or ceramic resonator is connected. When using a resonator, connect it as close as possible. Leave it open when not in use.	H
17	XT	I	Positive	Crystal or ceramic resonator connection pin. A feedback resistor of about 1MΩ is built in between the XT pin and the XTB pin. To use an external clock, input from this pin. Delete the capacitor when a crystal or ceramic resonator is connected. When using a resonator, connect it as close as possible. Leave it open when not in use.	L
19	DV_{DD}	P	-	Digital power supply pin. Connect a bypass capacitor between this pin and the DGND pin.	—
20	V_{DDL}	O	-	2.5V regulator output pin. Used as internal power supply. Connect a capacitor between this pin and DGND pin as close as possible.	L
21	SG	O	-	Reference voltage output pin for the built-in speaker amplifier. Connect a capacitor between this pin and SPGND pin.	L
22	AIN	I	-	Speaker amplifier analog signal input pin. Initially, input is disabled.	L
23	SPV_{DD}	P	-	Power supply pin for speaker amplifier. Connect a bypass capacitor between this pin and the SPGND pin.	—
24	SPGND	G	-	Speaker amplifier ground pin.	—
26	SPP	O	-	Positive output pin of the speaker amplifier. Line amplifier outputs are also available with AMODE command.	L
27	SPM	O	-	Negative output pin of the speaker amplifier.	Hi-Z

*1 Initial value at reset input and power-down. The pin whose IO is "I" indicates a fixed level from outside.

Pin	Symbol	I/O	Attribute	Description	Initial value *1
28	RESETB	I	Negative	Reset input pin. The LSI is initialized by the "L" level input. After a reset is input, all the circuits stop operating and enter the power-down state. At power-on, input an "L" level to this pin. After the power supply voltage stabilizes, set this pin to an "H" level. A pull-up resistor is internally connected.	(*2)
29	TEST0	I	Positive	Input pin for testing. A pull-down resistor is internally connected. Fix to the DGND.	L
30	STATUS1	O	-	Status/error output pin 1. Execute OUTSTAT command to select BUSYB*3 and NCR*3 in each channel, or errors. The initial value is BUSYB*3 of channel 0, and output data is "H" level.	H
31	STATUS2	O	-	Status/error output pin 2. Execute OUTSTAT command to select BUSYB*3 and NCR*3 in each channel, or errors. The initial value is BUSYB*3 of channel 0, and output data is "H" level.	H
32	CBUSYB	O	Negative	Command processing status signal output pin. An "L" level is output during command processing. Be sure to input a command with this pin at an "H" level.	(*2)
2,8, 15,25	N.C.	-	-	Unused pin. Leave open.	Hi-Z

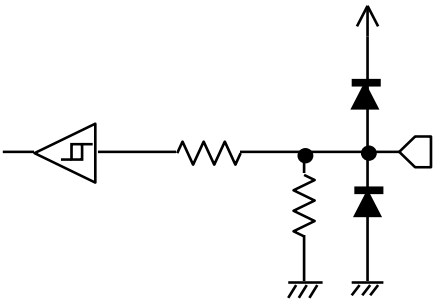
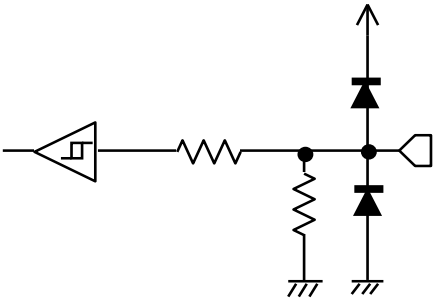
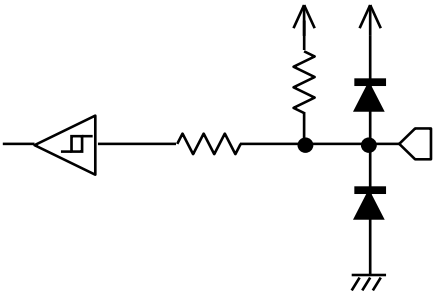
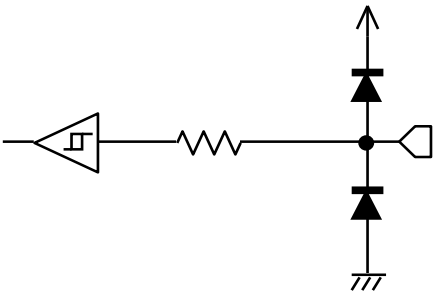
*1 Initial value at reset input and power-down. The pin whose IO is "I" indicates a fixed level from outside.
*2 "L" at reset, "H" at power-down
*3 For NCR, BUSYB, refer to the description of "RDSTAT command".

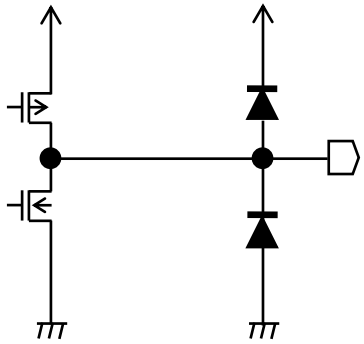
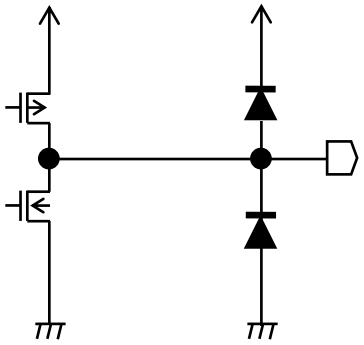
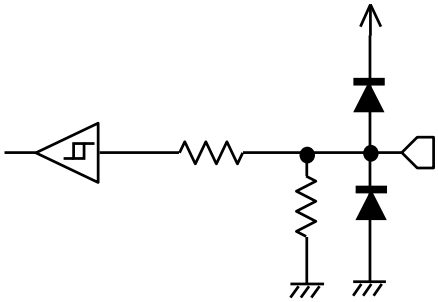
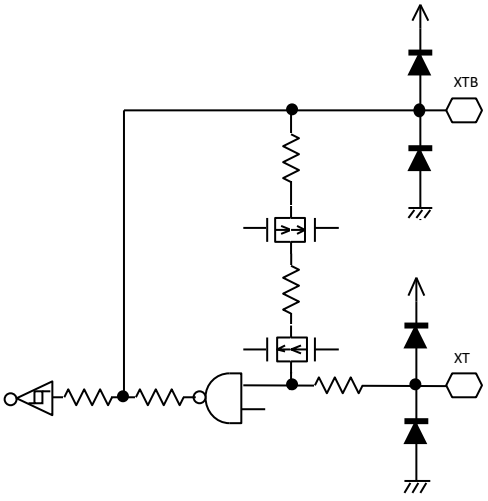
■ Termination of Unused Pins

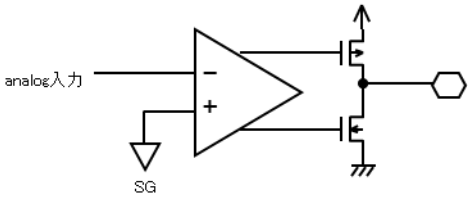
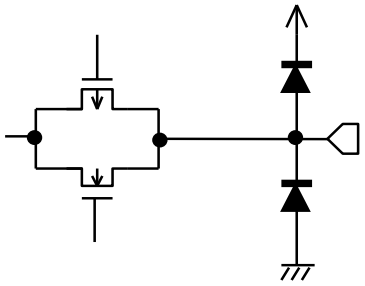
This section explains how to terminate unused pins.

Symbol	Recommended pin termination
EROFF	Connect to the DGND.
XT	Leave open.
XTB	
AIN	Connect to the SPGND.
TEST0	Connect to the DGND.
N.C.	Leave open.
SO	
SPM	
STATUS1	
STATUS2	

■ I/O Equivalent Circuit

Classification	Circuit	Overview
A		Attribute: Input Power: DV_{DD} Function: CMOS inputs with pull-down Applicable pin: TEST0
B		Attribute: Input Power: IOV_{DD} Function: CMOS inputs with pull-down Applicable pin: EROFF
C		Attribute: Input Power: DV_{DD} Function: CMOS inputs with pull-up Applicable pin: RESETB
D		Attribute: Input Power: DV_{DD} Function: CMOS inputs Applicable pins: SI, SCK, CSB

Classification	Circuit	Overview
F		Attribute: output Power: DV_{DD} Function: CMOS outputs Applicable pins: STATUS1, STATUS2, CBUSYB,SO
G		Attribute: output Power: IOV_{DD} Function: CMOS outputs Applicable pin: ERCSB, ERSCK, ERSO
H		Attribute: Input Power: IOV_{DD} Function: CMOS inputs with pull-down Applicable pin: ERSI
I		Attribute: Oscillator circuit Power: DV_{DD} Function: 4.096M, 4.000MHz oscillation Applicable pins: XT, XTB

Classification	Circuit	Overview
J		Attribute: Analog Power: SPV_{DD} Function: Sound output Applicable pins: SPP, SPM
L		Attribute: Analog Power: SPV_{DD} Function: Sound input Applicable pins: AIN

■ Electrical characteristics

● Absolute maximum rating

DGND=SPGND=0V, Ta=25°C

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	DV_{DD} IOV_{DD} SPV_{DD}	—	-0.3 to +6.0	V
Input voltage 1	V_{IN1}	—	-0.3 to DV_{DD}+0.3	V
Input voltage 2	V_{IN2}	—	-0.3 to IOV_{DD}+0.3	V
Allowable loss	P_D	When the LSI is mounted on JEDEC 4-layer board. SPV_{DD} = 5V	1000	mW
Output short-circuit current	I_{OS}	Applies to pins other than SPM, SPP and V_{DDL} pins.	10	mA
		Applies to SPM and SPP pins.	500	mA
		Applies to the V_{DDL} pin.	50	mA
Storage temperature	T_{STG}	—	-55 to +150	°C

● Recommended operating conditions

DGND=SPGND=0V

Parameter	Symbol	Condition	Range			Unit
DV_{DD}, IOV_{DD}, SPV_{DD}*1,Power-supply voltage	DV_{DD} IOV_{DD} SPV_{DD}	—	2.7 to 3.6 / 3.3 to 5.5			V
Operating temperature	Top	—	-40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			Typ -5%	4.096 4.000	Typ +5%	

*1 $SPV_{DD} \geq DV_{DD}$

- DC characteristics

$SPV_{DD} \geq DV_{DD} = IOV_{DD}$=2.7 to 5.5V, DGND=SPGND=0V, Ta=-40 to +85°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.*1	Max.	Unit
"H" input voltage 1	V_{IH1}	—	CSB/SCK/SI/ XT/RESETB/TEST0	0.8×DV_{DD}	—	DV_{DD}	V
"H" input voltage 2	V_{IH2}	—	ERSI/EROFF	0.8×IOV_{DD}	—	IOV_{DD}	V
"L" input voltage 1	V_{IL1}	—	CSB/SCK/SI/ XT/RESETB/TEST0	0	—	0.2×DV_{DD}	V
"L" input voltage 2	V_{IL2}	—	EROFF/ERSI	0	—	0.2×IOV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = -50µA	XTB	DV_{DD}-0.4	—	—	V
"H" output voltage 2	V_{OH2}	I_{OH} = -1mA	SO/ CBUSYB/STATUS1/ STATUS2	DV_{DD}-0.4	—	—	V
"H" output voltage 3	V_{OH3}	I_{OH} = -1mA	ERCSB/ERSCK/ ERSO	IOV_{DD}-0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 50µA	XTB	—	—	0.4	V
"L" output voltage 2	V_{OL2}	I_{OL} = 2mA	SO/ CBUSYB/STATUS1/ STATUS2	—	—	0.4	V
"L" output voltage 3	V_{OL3}	I_{OL} = 2mA	ERCSB/ERSCK/ ERSO	—	—	0.4	V
Output leakage current 1	I_{OOH1}	VOH=DV_{DD} (in high-impedance state)	SO	—	—	10	µA
	I_{OOL1}	VOL=DGND (in high-impedance state)		–10	—	—	µA
Output leakage current 2	I_{OOH2}	VOH=IOV_{DD} (in high-impedance state)	ERCSB/ERSCK/ ERSO	—	—	10	µA
	I_{OOL2}	VOL=DGND (in high-impedance state)		–10	—	—	µA
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	XT	0.8	5.0	20	µA
"H" input current 2	I_{IH2}	V_{IH} = DV_{DD}	RESETB/ CSB/SCK/SI	—	—	10	µA
"H" input current 3	I_{IH3}	V_{IH} = DV_{DD}	TEST0	20	500	1000	µA
"H" input current 5	I_{IH5}	V_{IH} = IOV_{DD}	EROFF	20	500	1000	µA
"H" input current 6	I_{IH6}	V_{IH} = IOV_{DD}	ERSI	2	100	400	µA
"L" input current 1	I_{IL1}	V_{IL} = DGND	XT	–20	–5.0	–0.8	µA
"L" input current 2	I_{IL2}	V_{IL} = DGND	CSB/SCK/SI/ EROFF/ TEST0	–10	—	—	µA
"L" input current 3	I_{IL3}	V_{IL} = DGND	RESETB	–400	–100	–2	µA
During playback Current consumption	I_{DDO}	f_{OSC}=4.096MHz Fs=48kHz, f=1kHz, During HQADPCM playback SPP/SPM No output load	—	—	25*2	45*2	mA
Power-down Current consumption	I_{DDS}	Ta=-40 to +55°C	—	—	1*2	10.0*2	µA
		Ta=-40 to +85°C	—	—	1*2	30.0*2	µA

*1 Typ. : DV_{DD}=SPV_{DD}=IOV_{DD}=5.0V,DGND=SPGND=0 V,Ta=25°C

*2 Total values of the DV_{DD} pin, SPV_{DD} pin, and IOV_{DD} pin

- Analog Part Characteristics

$SPV_{DD} \geq DV_{DD} = IOV_{DD}$=2.7 to 5.5V, DGND=SPGND=0V, Ta=-40 to +85°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RC4MHz clock frequency	Frc	Ta=-40 to +70°C	3.89	4.096	4.31	MHz
		Ta=-40 to +85°C	3.68	4.096	4.51	MHz
AIN pin input resistance	R_{AIN}	Input gain 0dB	10	20	30	kΩ
AIN pin input voltage range	V_{AIN}	—	—	—	SPV_{DD}×2/3	Vp-p
Line amplifier output resistance1*1	R_{LA1}	SPV_{DD} = 3.3 to 5.5V When 1/2SPV_{DD} ± 1 mA is applied	—	—	100	Ω
Line amplifier output resistance2*1	R_{LA2}	SPV_{DD} = 2.7 to 3.6V When 1/2SPV_{DD} ± 1 mA is applied	—	—	300	Ω
Line amplifier output-load-resistance *1	R_{LA}	For SPGND	10	—	—	kΩ
Line amplifier Out put Voltage Range *1	V_{AO}	No output load	SPV_{DD} /6	—	SPV_{DD}×5/6	V
SG pin output voltage	V_{SG}	—	0.95x SPV_{DD} /2	SPV_{DD} /2	1.05x SPV_{DD} /2	V
SG pin output resistance	R_{SG}	—	57	96	135	kΩ
SPP/SPM pins Output-Load Resistance	R_{LSP1}	—	6	8	—	Ω
To the SPP and SPM pins Short circuit detection	R_{OCDAB}	Class AB speaker amplifier 4.5V≤SP_{VDD}≤5.5V	0.1	—	6	Ω
	R_{OCDD}	Class D speaker amplifier 4.5V≤SP_{VDD}≤5.5V	0.1	—	3	Ω
Speaker amplifier output power 1	P_{SPO1}	SPV_{DD} =5.0V, f=1kHz R_{SPO}=8Ω, THD=10%	0.8	1	—	W
Speaker amplifier output power 2	P_{SPO2}	SPV_{DD} =3.0V, f=1kHz R_{SPO}=8Ω, THD=10%	0.1	0.3	—	W
During no-signal SPM-SPP Output offset voltage	V_{OF}	AVOL=0dB 8 Ω load	-50	—	50	mV

*1 Applies to the SPP when outputting LINE.

- AC characteristic

$SPV_{DD} \geq DV_{DD} = IOV_{DD}$=2.7 to 5.5V, DGND=SPGND=0V, Ta=-40 to +85°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle	f_{duty}	—	40	50	60	%
RESETB input pulse width	t_{RST}	—	10	—	—	µs
Reset noise rejection pulse width	t_{NRST}	RESETB pin	—	—	0.1	µs
Command input interval time	t_{INTC}	f_{OSC} = 4.096MHz After input the first command at two-times command input mode	0	—	—	µs
Command input enable time	t_{cm}	f_{OSC} = 4.096MHz During continuous playback at SLOOP input	—	—	10	ms
At PUP command input CBUSYB "L" level output time	t_{PUP}	4.096MHz external clock input	—	—	8	ms
At AMODE command input CBUSYB "L" level output time	t_{PUPA1}	4.096MHz external clock input POP="L" AEN0="L"→"H" AEN1 = "L" AVOL = -4dB is selected	35	37	39	ms
At AMODE command input CBUSYB "L" level output time	t_{PUPA2}	4.096MHz external clock input DAMP="L",POP="H" AEN1="L"→"H"	71	73	75	ms
At AMODE command input CBUSYB "L" level output time	t_{PUPA3}	4.096MHz external clock input DAMP="L",POP="L" AEN1="L"→"H"	31	33	35	ms
At PDWN command input CBUSYB "L" level output time	t_{PD}	f_{OSC} = 4.096MHz	—	—	10	µs
At AMODE command input CBUSYB "L" level output time	t_{PDA1}	4.096MHz external clock input POP="L" AEN1="L",AEN0="H"→"L"	100	102	104	ms
At AMODE command input CBUSYB "L" level output time	t_{PDA2}	4.096MHz external clock input DAMP="L",POP="H" AEN1="H"→"L"	142	144	146	ms
At AMODE command input CBUSYB "L" level output time	t_{PDA3}	4.096MHz external clock input DAMP="L",POP= "L" AEN1="H"→"L"	102	104	106	ms
CBUSYB "L" level output time 1[*1]	t_{CB1}	f_{OSC} = 4.096MHz	—	—	10	µs
CBUSYB "L" level output time 2[*2]	t_{CB2}	f_{OSC} = 4.096MHz	—	—	3	ms
CBUSYB "L" level output time 3[*3]	t_{CB3}	FAD="L" at f_{OSC} = 4.096MHz	—	—	200	µs
		FAD="H" at f_{OSC} = 4.096MHz	—	—	10	ms

*1 Applies when inputting commands except the timings after PUP, PDWN, PLAY, or START command is input.

*2 Applies when inputting PLAY, START, MUON command.

*3 Applies when inputting STOP command.

- AC Characteristics (Clock Synchronous Serial Interface)

SPV_{DD} ≥DV_{DD}=IOV_{DD}=2.7 to 5.5V, DGND=SPGND=0V, Ta=-40 to +105°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSB input enable time from EROFF falling edge	t_{EEROFF}	—	1000	—	—	ns
CSB hold time from EROFF rising edge	t_{EROFFH}	—	1000	—	—	ns
SCK setup time from CSB falling edge	t_{SCKS}	—	100	—	—	ns
SCK input enable time from CSB falling edge	t_{ESCK}	—	100	—	—	ns
SCK hold time from CSB rising edge	t_{CSH}	—	100	—	—	ns
Data floating time from CSB rising edge	t_{DOZ}	RL=3KΩ	—	—	100	ns
Data setup time from SCK	t_{DIS}	—	50	—	—	ns
Data hold time from SCK	t_{DIH}	—	50	—	—	ns
Data output delay time from SCK	t_{DOD}	—	—	—	90	ns
LSB data hold time from SCK	t_{DOH}	—	100	—	—	ns
SCK "H" level pulse width	t_{SCKH}	—	100	—	—	ns
SCK "L" level pulse width	t_{SCKL}	—	100	—	—	ns
CBUSYB output delay time from SCK	t_{DBSY}	—	—	—	90	ns

<When rewriting the flash memory using the clock synchronous serial interface>

SPV_{DD} ≥DV_{DD}=IOV_{DD}=2.7 to 5.5V, DGND=SPGND=0V, Ta=-40 to +105°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSB input enable time from EROFF falling edge	t_{EEROFF}	—	1000	—	—	ns
CSB hold time from EROFF rising edge	t_{EROFFH}	—	1000	—	—	ns
SCK setup time from CSB falling edge	t_{SCKS}	—	125	—	—	ns
SCK input enable time from CSB falling edge	t_{ESCK}	—	125	—	—	ns
SCK hold time from CSB rising edge	t_{CSH}	—	125	—	—	ns
Data floating time from CSB rising edge	t_{DOZ}	RL=3KΩ	—	—	125	ns
Data setup time from SCK	t_{DIS}	—	50	—	—	ns
Data hold time from SCK	t_{DIH}	—	50	—	—	ns
Data output delay time from SCK	t_{DOD}	—	—	—	110	ns
LSB data hold time from SCK	t_{DOH}	—	100	—	—	ns
SCK "H" level pulse width	t_{SCKH}	—	125	—	—	ns
SCK "L" level pulse width	t_{SCKL}	—	125	—	—	ns

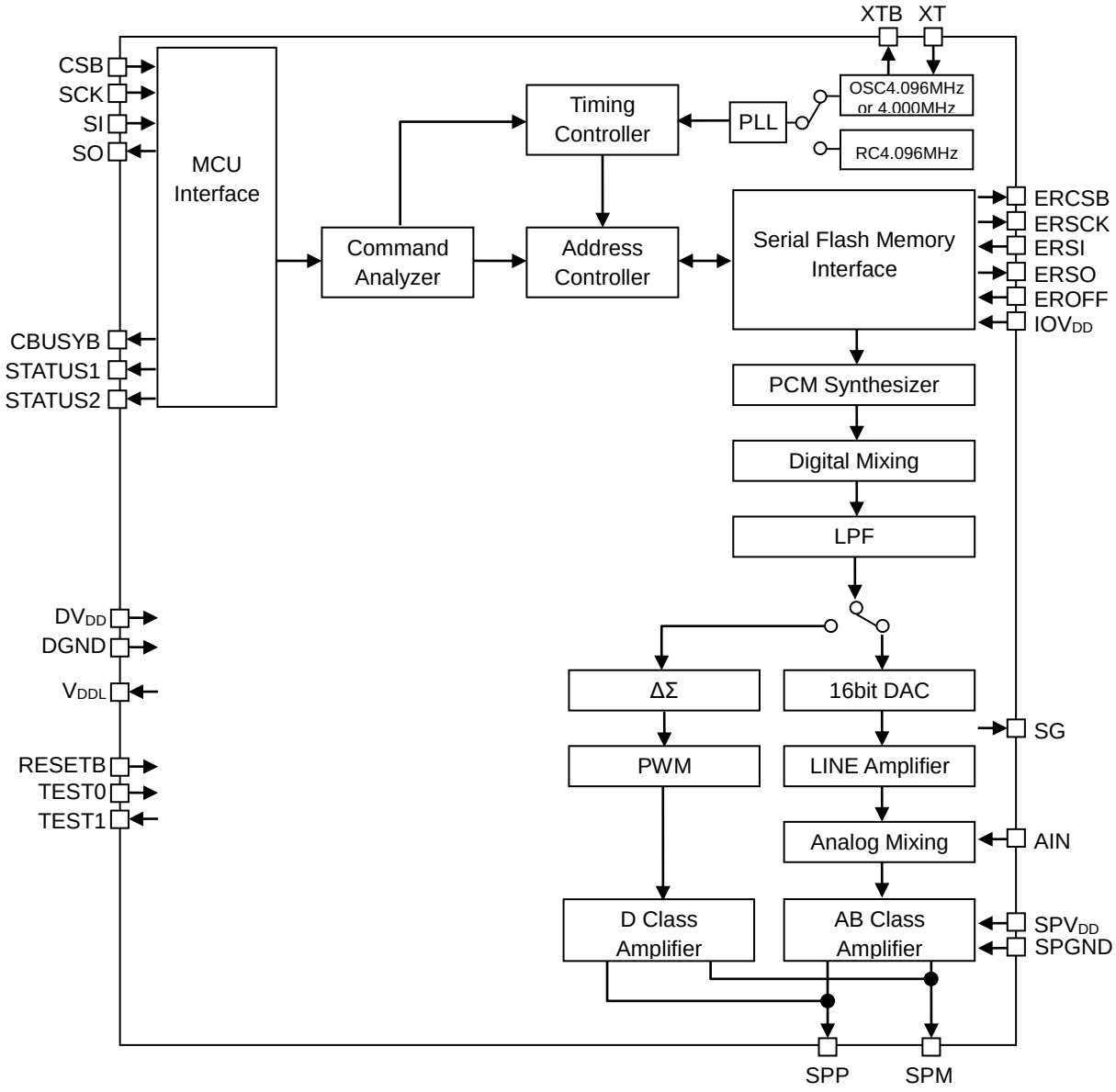
- AC Characteristics (Flash Memory Interface)

$SPV_{DD} \geq DV_{DD}=IOV_{DD}$=2.7 to 5.5V, DGND=SPGND=0V, Ta=-40 to +85°C, Load capacitance of output pin =15pF(max.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
ERSCK enable time from ERCSB falling edge	t_{ECSS}	—	50	—	—	ns
ERSCK hold time from ERCSB rising edge	t_{ECSH}	—	50	—	—	ns
Data setup time from ERSCK rising edge	t_{EDIS}	—	10	—	—	ns
Data hold time from ERSCK rising edge	t_{EDIH}	—	10	—	—	ns
Data delay time from ERSCK falling edge	t_{EDOD}	—	—	—	5	ns
ERSCK frequency	t_{ESCKF}	—	1.228	16.384	17.20	MHz
ERSCK "H" level pulse width	t_{ESCKH}	—	26	—	—	ns
ERSCK "L" level pulse width	t_{ESCKL}	—	26	—	—	ns
ERCSB/ERSC/ERSO delay time from EROFF rising edge	t_{EFLH}	—	—	—	1	ms
ERCSB/ERSC/ERSO delay time from EROFF falling edge	t_{EFHL}	—	—	—	1	ms

■ Block diagram

The block diagram is shown below.

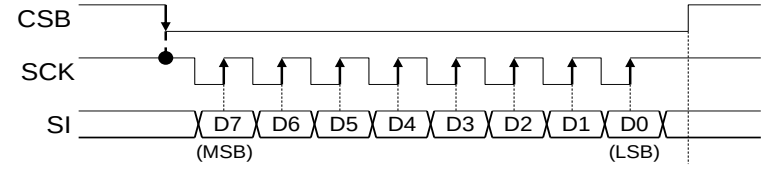


■ Function description

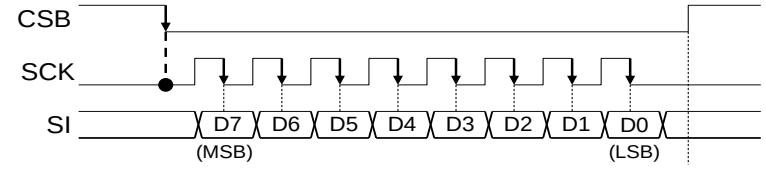
- Clock Synchronous Serial Interface

The CSB, SCK, SI, and SO pins are used to input various command data and to read the status.
For command and data inputting, after "L" level is input to the CSB pin, data is input to the SI pin in MSB first in synchronization with the input clock signal of the SCK pin. The SI pin data is loaded into the LSI in synchronization with the SCK pin clock, and the command data is determined by the SCK pin clock of the eighth pulse.
When reading, after "L" level is input to the CSB pin, it is output from the SO pin in synchronization with the input clock signal of the SCK pin.
The selection of the rising or falling edge of the SCK pin clock depends on the state of the SCK pin at the falling edge of the CSB pin.
When the SCK pin is "H" at the falling edge of the CSB pin, the SI pin data is loaded into the LSI on the rising edge of the SCK pin clock, and the status signal is output from the SO pin on the falling edge of the SCK pin clock.
When the SCK pin is "L" at the falling edge of the CSB pin, the SI pin data is loaded into the LSI on the falling edge of the SCK pin clock, and the status signal is output from the SO pin on the rising edge of the SCK pin clock.
When the CSB pin is fixed to "L" level, the SI pin data is loaded into the LSI on the rising edge of the SCK pin clock, and the status signal is output from the SO pin at the falling edge of the SCK pin clock.
However, if unexpected pulses are input to the SCK pin due to noise, etc., the count of the number of SCK pin clocks may be shifted, and normal command input may not be performed.
The serial interface can be returned to the initial state by setting the CSB pin to "H" level.
When the CSB pin is "H" level, the SO pin becomes a high impedance state.

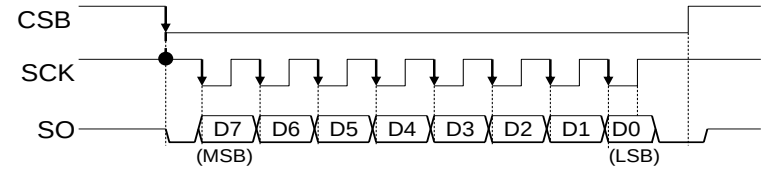
Command data input timing: SCK rising edge operation
(When the SCK is "H" at the falling edge of the CSB)



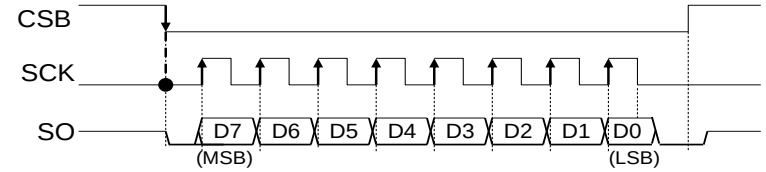
Command data input timing: SCK falling edge operation
(When the SCK is "L" at the falling edge of the CSB)



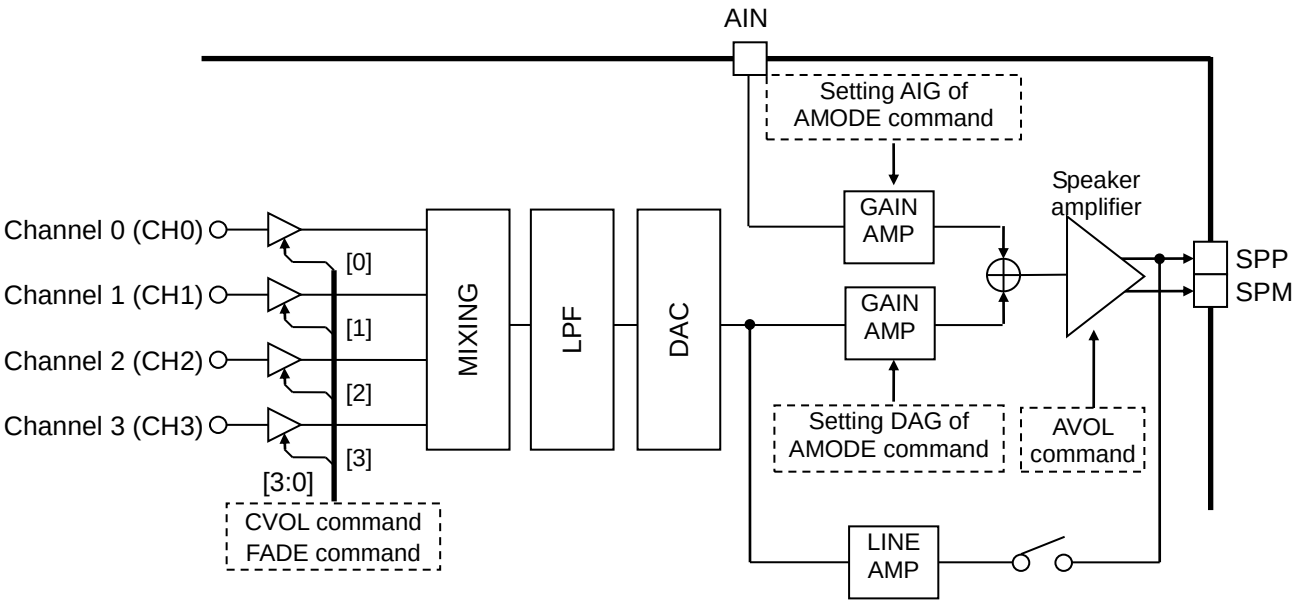
Command data output timing: SCK falling edge operation
(When the SCK is "H" at the falling edge of the CSB)



Command data output timing: SCK rising edge operation
(When the SCK is "L" at the falling edge of the CSB)



- Volume Settings (Differences Between AVOL and CVOL)
  The volume can be set with 3 commands CVOL, AVOL and AMODE.
  The CVOL can set the volume of each channel, the AVOL can set the volume after channel mixing, and the AMODE can set the input gain to the amplifier. By using the fade function with FADE command, the volume can be adjusted stepwise when the volume is changed with CVOL.



- Speech synthesis algorithm

  This LSI contains five algorithm types to match the characteristic of playback sound: 4-bit ADPCM2 algorithm, HQ-ADPCM algorithm, 8-bit non-linear PCM algorithm, 8-bit straight PCM algorithm, and 16-bit straight PCM algorithm. Key feature of each algorithm is described in the table below.

Speech synthesis algorithm	Compression rate*1	Feature
HQ- ADPCM	1/5	4bit ADPCM algorithm is improved. Adopting variable bit length enables high sound quality and high data compression. Suitable for sound effects with sharp changes in waveforms or for pulsed waveforms.
4-bit ADPCM2	1/4	LAPIS original 4bit ADPCM algorithm is improved. Better followability to the waveform improves the sound quality. Suitable for human voices, animal crying, and natural sounds.
8-bit non-linear PCM	1/2	This algorithm enables playing back a sound with 10-bit equivalent quality in the center of the waveform. Suitable for low-amplitude sounds that are easily distorted.
8-bit straight PCM	1/2	This algorithm has excellent followability to the waveform in all sound areas. Suitable for sound effects with sharp changes in waveforms or for pulsed waveforms.
16-bit straight PCM	1	This algorithm has excellent followability to the waveform in all sound areas. Suitable for sound effects with sharp changes in waveforms or for pulsed waveforms.

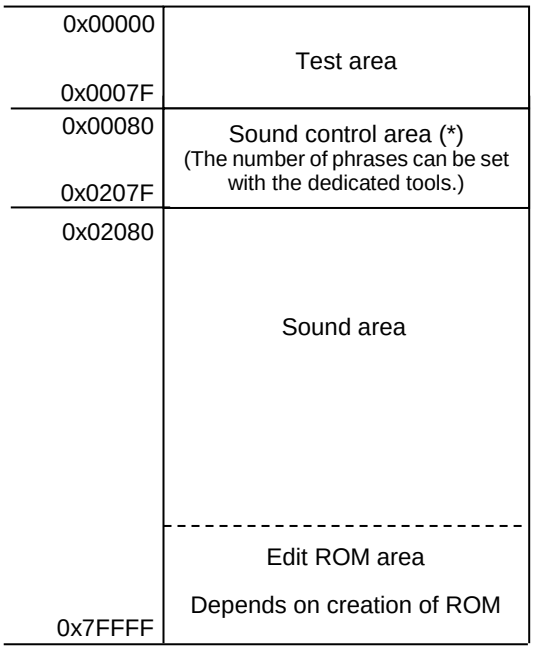
*1: When using the same sampling frequency.

- Memory Allocation and Creating Sound Data

  The serial flash memory is partitioned into four data areas: sound (i.e., phrase) control area, test area, sound area, and edit ROM area.
  The sound control area manages the sound data in the ROM. It contains data for 4,096 phrases.
  The sound area contains actual waveform data.
  The edit ROM area contains data for effective use of sound data. For the details, refer to the section of "Edit ROM Function".
  The edit ROM area is not available if the edit ROM is not used.

  The ROM data is created using a dedicated tool (Speech LSI Utility).

Configuration of Serial Flash Memory Data (4Mbit)



(*) When the number of phrases is set to 1024
The number of phrases can be set from 1024 to 4096 in 1024 units using the dedicated tools.

- Playback time and memory capacity

  The playback time depends on the number of phrases, memory capacity, sampling frequency, and playback algorithm. The relationship is shown below. However, this is the playback time when the edit ROM function is not used.

$$\text{Playback Time} = \frac{1.024 \times (\text{Memory Capacity (kbit)} - (0.0625 \times \text{Number of Phrases}) - 0.625)}{\text{Sampling frequency (kHz)} \times \text{bit length}} \quad \text{(sec)}$$

  When the number of phrases is 1024, the sampling frequency is 16kHz, and the HQ-ADPCM algorithm is selected, the playback time will be approximately 81 seconds.

$$\text{Playback Time} = \frac{1.024 \times (4096(\text{kbit}) - (0.0625 \times 1024) - 0.625)}{16\ (\text{kHz}) \times 3.2\ (\text{bit})\ (\text{average})} \fallingdotseq 81\ (\text{sec})$$

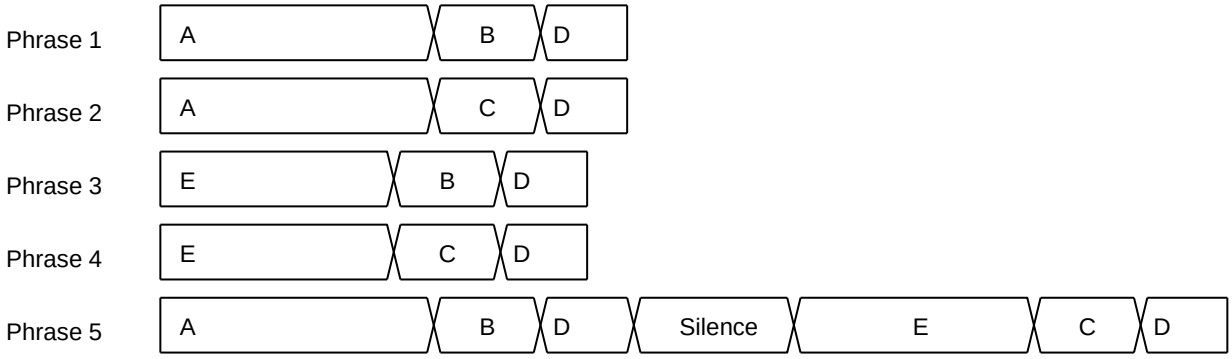
- Edit ROM Function

  With the edit ROM function, multiple phrases can be played in succession. The following functions can be configured using the edit ROM function:

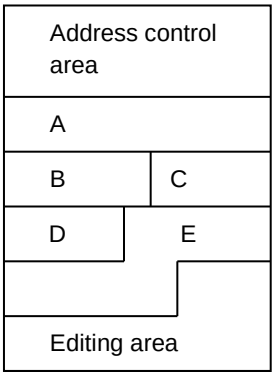
  - Continuous playback: There is no limit to the continuous playback count that can be specified. It depends on the memory capacity only.
  - Silence insertion: 20 to 1024 ms

  Using the edit ROM function enables an effective use of the flash memory capacity.
  Below is an example of the ROM configuration in the case of using the edit ROM function.

Examples of Phrases Using the Edit ROM Function



Example of ROM Data Where the Contents Above Are Stored in ROM

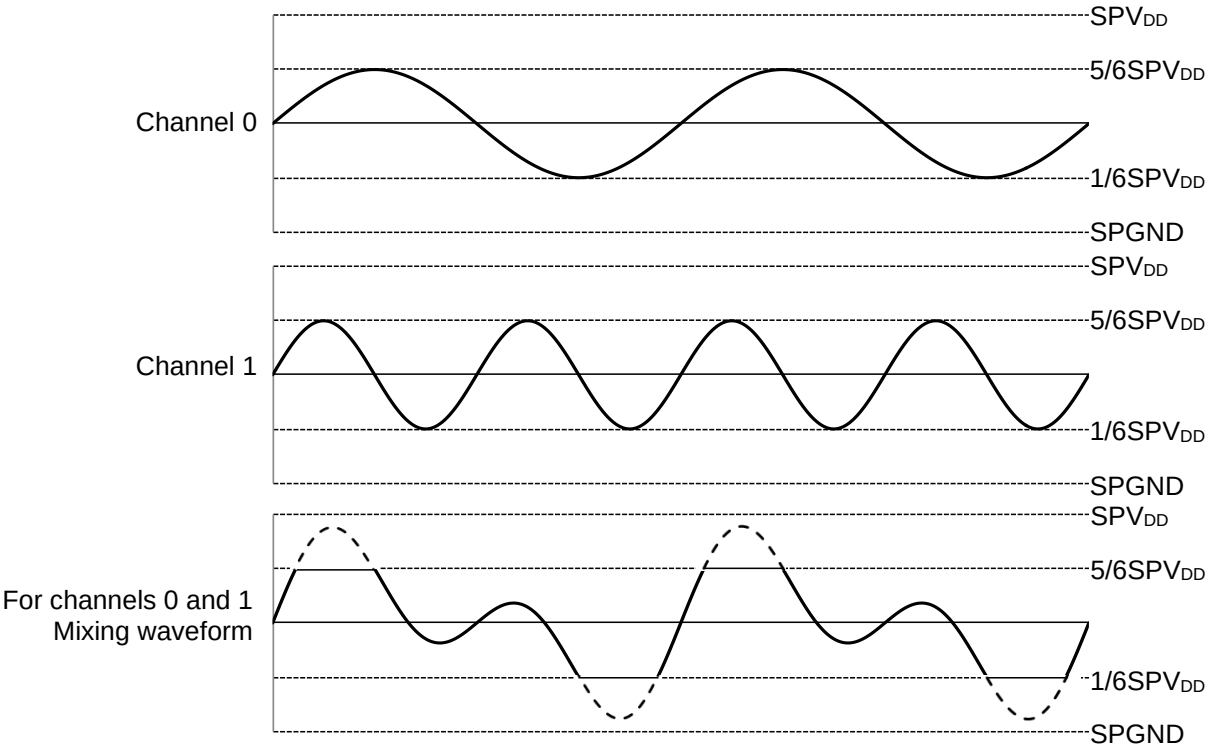


- Mixing function

  Up to 4 channels mixing playback is possible at the same time. Commands with channel designation can set channels independently.

◆ Waveform clamp precautions for mixing

When mixing, the clamp may be generated as shown in the figure below due to the calculation of the synthesis. If the clamp is known to be generated in advance, adjust the volume of each channel by CVOL command.



If the result of mixing channels 0 and 1 exceeds from the $1/6SPV_{DD}$ to 5/6SPVDD level (as indicated by the broken line), the sound quality may be reduced by clamping.
Waveforms when AVOL is set to 0.0dB.

◆ Class D amplifier precaution on mixing

When mixing with a class d amplifier, use the CVOL command to adjust the volume so that the waveform after mixing does not exceed the full amplitude.

An example of adjusting the volume of the CVOL command during mixing playback is shown below.

Example1)
When performing 2-channels mixing playback of channel 0 and channel 1.

CVOL command setting value (CV1,CV0,CV6-CV2)		Description
Channel 0	Channel 1	
4Fh(-6.02dB)	4Fh(-6.02dB)	Set both channel 0 and channel 1 amplitude to 0.5x.
67h(-2.50dB)	37h(-12.04dB)	Set channel 0 amplitude to 0.75x and channel 1 amplitude to 0.25x.

Example2)
When performing 3-channels mixing playback of channel 0, channel 1 and channel 2.

CVOL command setting value (CV1,CV0,CV6-CV2)			Description
Channel 0	Channel 1	Channel 2	
15h(-9.83dB)	15h(-9.83dB)	15h(-9.83dB)	Set channel 0, channel 1 and channel 2 amplitude to 0.33x.
4Fh(-6.02dB)	37h(-12.04dB)	37h(-12.04dB)	Set channel 0 amplitude to 0.5x and channel 1 and channel 2 amplitude to 0.25x.

Example3)
When performing all channels mixing playback.

CVOL command setting value (CV1,CV0,CV6-CV2)				Description
Channel 0	Channel 1	Channel 2	Channel 3	
37h(-12.04dB)	37h(-12.04dB)	37h(-12.04dB)	37h(-12.04dB)	Set all channels amplitude to 0.25x.

Short detection of SPP pin and SPM pin always operates while using the class D amplifier. If the volume of CVOL command is adjusted incorrectly and it it is played back in the clamped state, the short detection circuit is determaine that a short has occurred.
When using class D amplifier, enable short detection of SPP pin and SPM pin by SAFE command and check the short detection error (SPDERR). Refer to SAFE command for setting.

◆ Different sampling frequency mixing algorithm

It is not possible to perform channel mixing by a different sampling frequency group.

Note that when channel synthesis is performed on a sampling frequency group other than the selected sampling frequency group, playback will be faster or slower.
The following table lists the frequency group that can be used when mixing different sampling frequency groups.

6.4kHz, 12.8kHz, 25.6kHz	... (Group 1)
8.0kHz, 16.0kHz, 32.0kHz	... (Group 2)
11.025kHz, 22.05kHz, 44.1kHz	... (Group 3)
12.0kHz, 24.0kHz, 48.0kHz	... (Group 4)
10.7kHz, 21.3kHz	... (Group 5)

The figure below shows the operation image when a sampling frequency group with different sampling frequency group is played back.

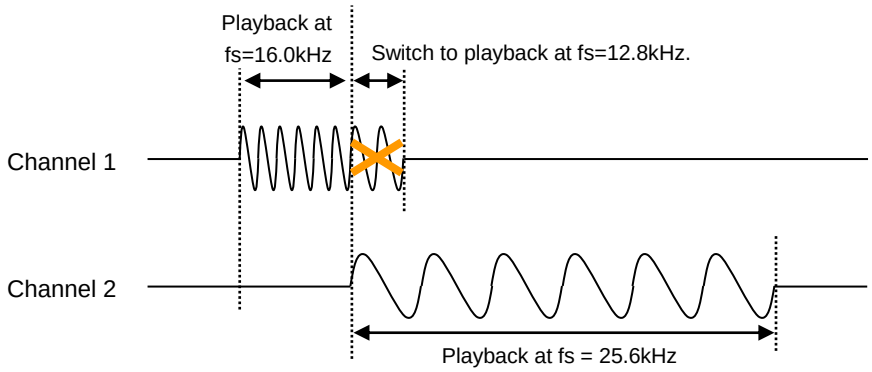


Figure 1) Case where a phrase is played at a sampling frequency belonging to a different sampling frequency group during playback on channels 1 and 2

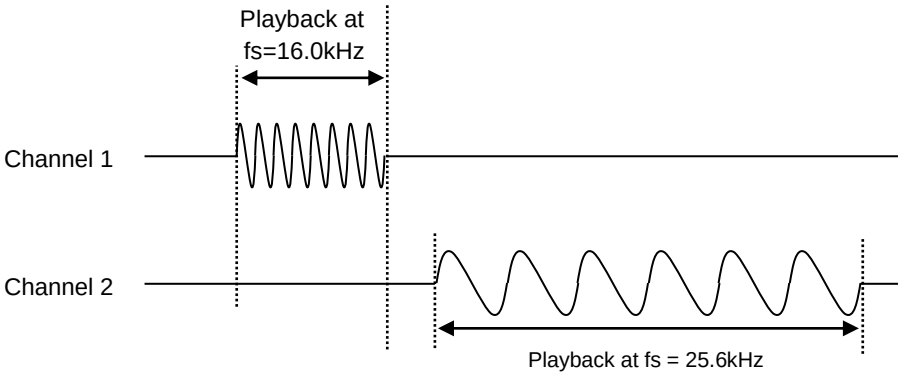


Figure 2) Case where a phrase is played at a sampling frequency belonging to a different sampling frequency group after playback is finished at the other channel

- Misoperation detection and failure detection functions

  Misoperation detection and failure detection functions can be set with SAFE command. The error detection status can be read by the RDERR command, and the error bit indicating the error detection status can be cleared by the ERRCL command. In addition, OUTSTAT command can be used to send whether an error is detected or not to the STATUS1 pin or STATUS2 pin. For SAFE, RDERR, ERRCL and OUTSTAT commands, refer to the "Command" section.
  Misoperation detection and failure detection are shown below.

  - Command error detection
  - Speaker disconnection detection
  - LSI temperature error detection
  - SPP pin and SPM pin short detection
  - Flash memory error detection
  - Watchdog timer overflow detection
  - RST counter overflow detection
  - Detects the stop of clock input from a crystal resonator or ceramic resonator.

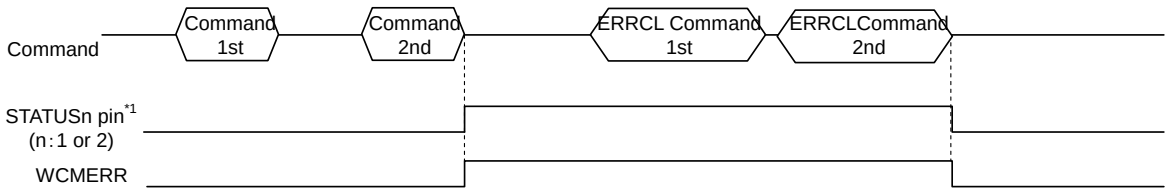
◆ Command error detection

This LSI detects two command errors: phrase number error and command error. Use the WCMEN bit of the SAFE command to set command error detection.

① Phrase number error.
Set the number of phrases (1024, 2048, 3072 or 4096) to use when creating sound data in the Speech LSI Utility. If you specify a phrase that exceeds the number of phrases specified by the Speech LSI Utility with the PLAY2 or FADR2 command, an error in the command is detected and the error bit (WCMERR) is set to "1".

② Command error.
This LSI has a function to input various commands and data two-times to prevent malfunction due to noise at the serial interface pin. The setting of the two-times input mode is made at power-up. Refer to the "PUP command" for the setting method.

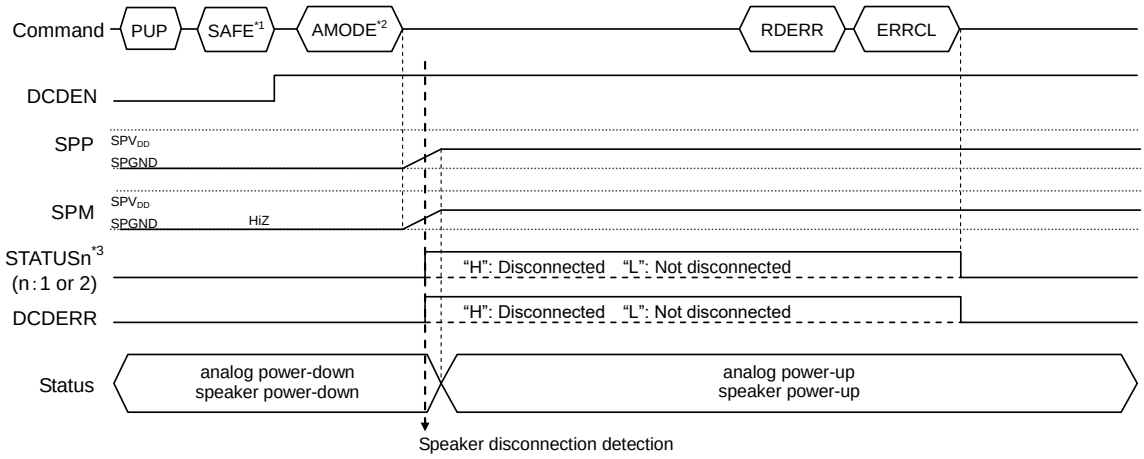
In the two-times input mode, the command data is input two-times in succession, and it is valid only when the input data matches. If a mismatch occurs during the second data input after the first data input, an error in the command is detected and the error bit (WCMERR) is set to "1", and the command entered is ignored.
Error bit (WCMERR) can be read with RDERR command. Also, error bit (WCMERR) can be cleared by ERRCL command.



*1 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

◆ Speaker disconnection detection

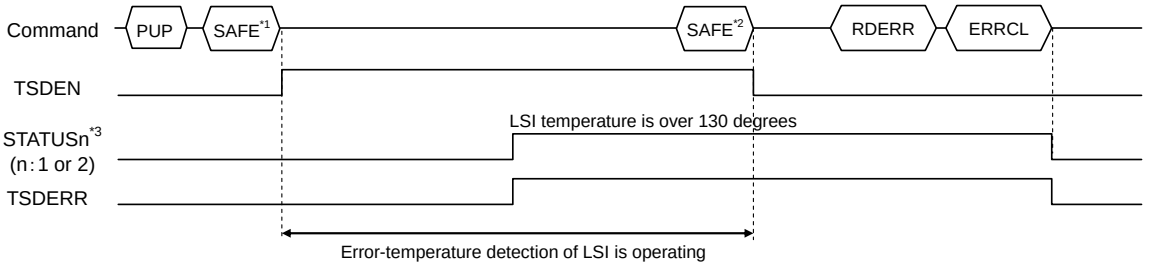
Set the speaker disconnection detection with the DCDEN bit of the SAFE command.
The speaker connection status of the SPP and SPM pins is checked when the analog power-up is activated in speaker amplifier output mode by AMODE command. When the disconnection of the speaker is detected, the error bit (DCDERR) is set to "1".
Error bit (DCDERR) can be read with RDERR command. Also, error bit (DCDERR) can be cleared by ERRCL command.



*1 Set DCDEN = "1"
*2 Analog power-up in speaker amplifier output mode
*3 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

◆ LSI temperature error detection

Set the LSI temperature error detection with the TSDEN bit of the SAFE command.
When the TSDEN bit is set to "1" by the SAFE command, LSI temperature error detection starts. When the TSDEN bit is set to "0", LSI temperature error detection ends.
When the LSI becomes 130^{O}C or more, the error bit (TSDERR) becomes "1".
Error bit (TSDERR) can be read with RDERR command. Also, error bit (TSDERR) can be cleared by ERRCL command.



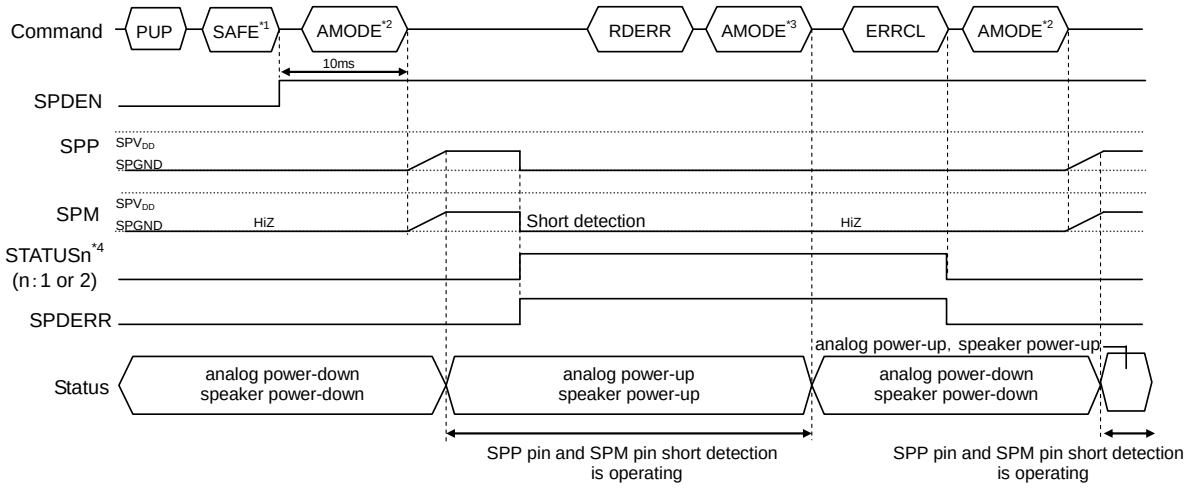
*1 Set TSDEN = "1"
*2 Set TSDEN = "0"
*3 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

◆ SPP pin and SPM pin short detection

Set the SPP pin and SPM pin short detection with the SPDEN bit of the SAFE command.
Detects short circuit between SPP pin and SPM pin, or SPP pin and GND (ground fault), or SPM pin and GND (ground fault). Can be used when $SPV_{DD} \geq 4.5V$. Operation is started by analog power-up in the speaker amplifier output mode by the AMODE command, and operation is terminated by power-down in the speaker amplifier output mode by the AMODE command.

After inputting SAFE command, start the analog power-up operation by AMODE command within 10ms.

When a short-circuit is detected, the error bit (SPDERR) is set to "1". When using a class D amplifier with the DAMP bit of AMODE command set to "1", if the PWM output is fixed to "H" level for 62.5us or longer, the error bit (SPDERR) is set to "1". At the same time, the speaker amplifier output pin (SPP/SPM) is forcibly turned off. Read the error bit (SPDERR) with the RDERR command, end playback, and perform analog power-down with the AMODE command. Then, use ERRCL command to clear the error bit (SPDERR).
To restart playback, use the AMODE command to analog power-up the speaker amplifier output mode and enter the PLAY command. However, if shorting to ground continues, the error bit (SPDERR) is set to "1" and the speaker amplifier output pin (SPP/SPM) is forcibly turned off simultaneously.
Short detection prevents damage to LSI. However, the detection circuit is effective in preventing damage due to unexpected accidents. It does not support continuous short operation or transient use.



*1 Set 1 SPDEN = "1"
*2 Analog power-up in speaker amplifier output mode
*3 Analog power-down in speaker amplifier output mode
*4 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

◆ Flash memory error detection

Set the Flash memory error detection with the ROMEN bit of the SAFE command. It is possible to detect two kinds of errors.

① Flash memory read data error

When an error is detected in the read data from the flash memory, the error bit (ROMERR) is set to "1". At the same time, playback of the corresponding channel is stopped.
If the error bit (ROMERR) is set to "1" after the PUP command and before the PLAY command or START command starts playback, this LSI may have error at the time of start. In such cases, initialize this LSI by moving the LSI to the power-down mode by resetting the LSI by the RESETB pin or by using PDWN command.

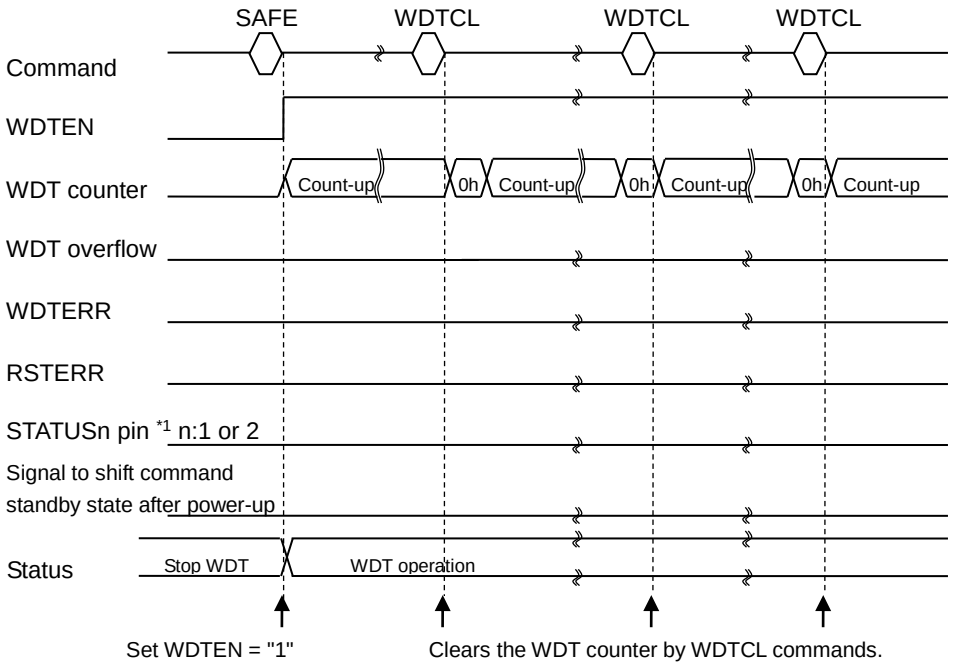
② Access outside the flash memory address range

If the flash memory is accessed outside the flash memory address range, an error is detected and the error bit (ROMERR) is set to "1".
At the same time, playback of the corresponding channel is stopped.

Error bit (ROMERR) can be read with RDERR command. Error bit (ROMERR) can be cleared by ERRCL command.

◆ Watchdog timer overflow detection

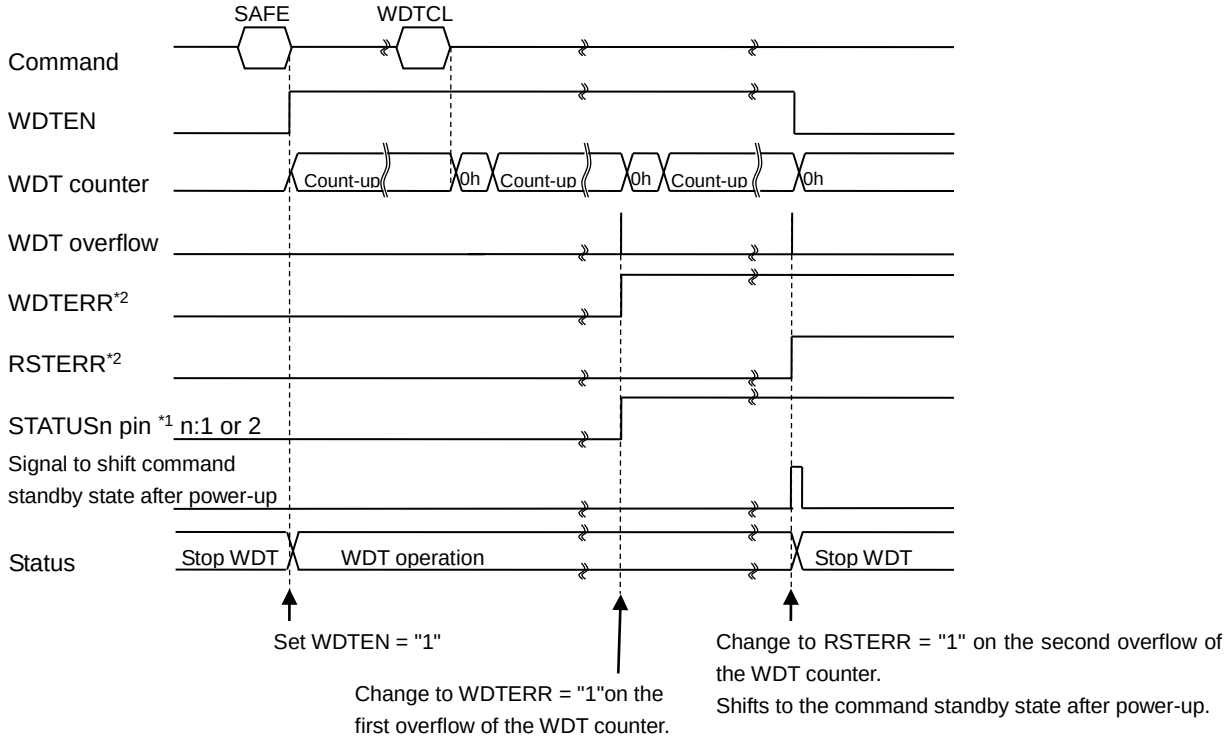
A communication error between the HOST MCU and this LSI (disconnection or short-circuit of the MCU command interface, etc.) can be detected.
Set the watchdog timer overflow detection with WDTEN bit of the SAFE command.
When the detection operation is started, the detection does not stop even if the WDTEN bit is set to "0".
After the detection operation starts, clear the WDT counter with the WDTCL command before the WDT counter overflows.
When the WDT counter overflows (for the first time), the error bit (WDTERR) is set to "1".
Error bit (WDTERR) can be read with RDERR command. In addition, the error bit (WDTERR) can be cleared by the ERRCL command after the WDTCL command.
The count time of the WDT counter is 2s the initial value. The counting time can be set to 125ms, 500ms, 2s, 4s. In addition, it is possible to shift to the command wait state after power-up by the second overflow of the WDT counter.
The count time and the second overflow operation can be set with the dedicated tools (Speech LSI Utility).



*1 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

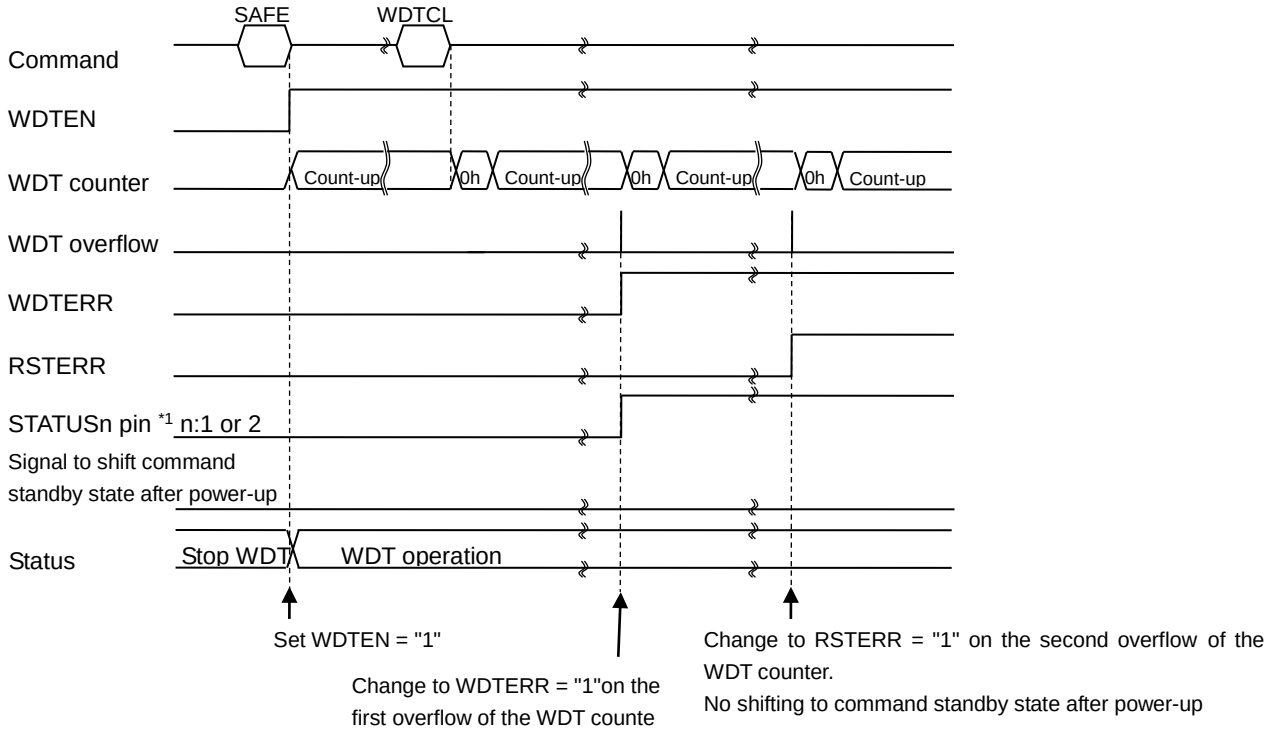
Recommended Operation Flow of Watchdog Timer

The operation when no WDTCL command is entered is as follows.
<When "Transition to the command standby state after power-up" is selected by the second overflow of the WDT counter>



*1 Misoperation detection and failure detection outputs are selected by OUTSTAT command.
*2 Even if transferring to the command standby state after power-up by the second overflow of the the WDT counter, the state of WDTERR bit and RSTERR bit remain. The state configured by OUTSTAT command also remains.

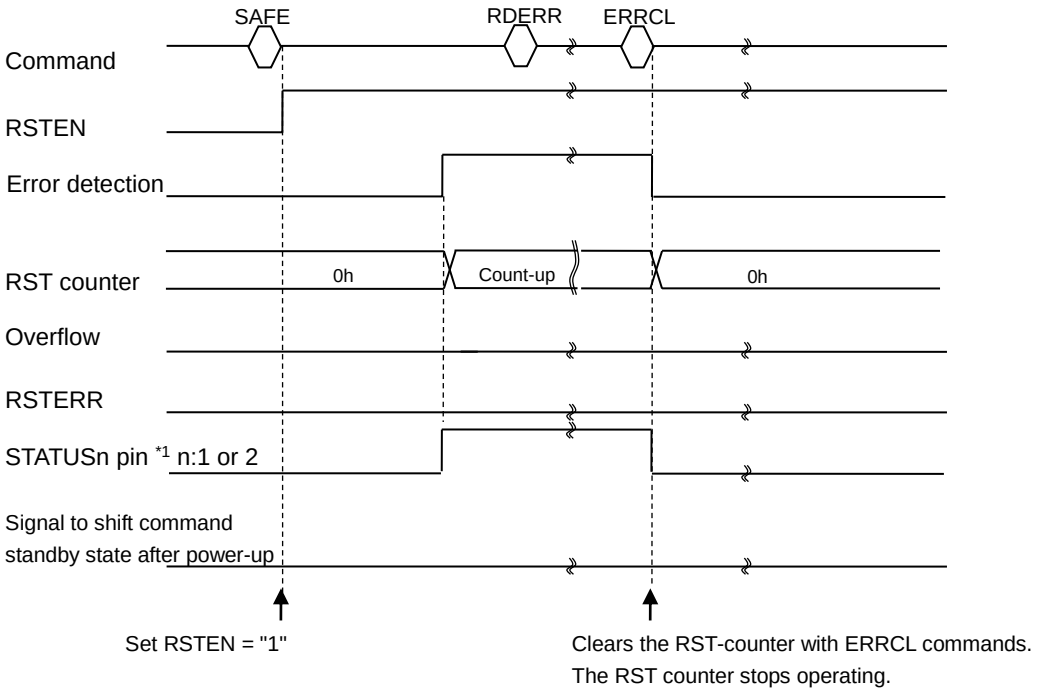
<When "Transition to the command standby state after power-up " is not selected by the second overflow of the WDT counter>



*1 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

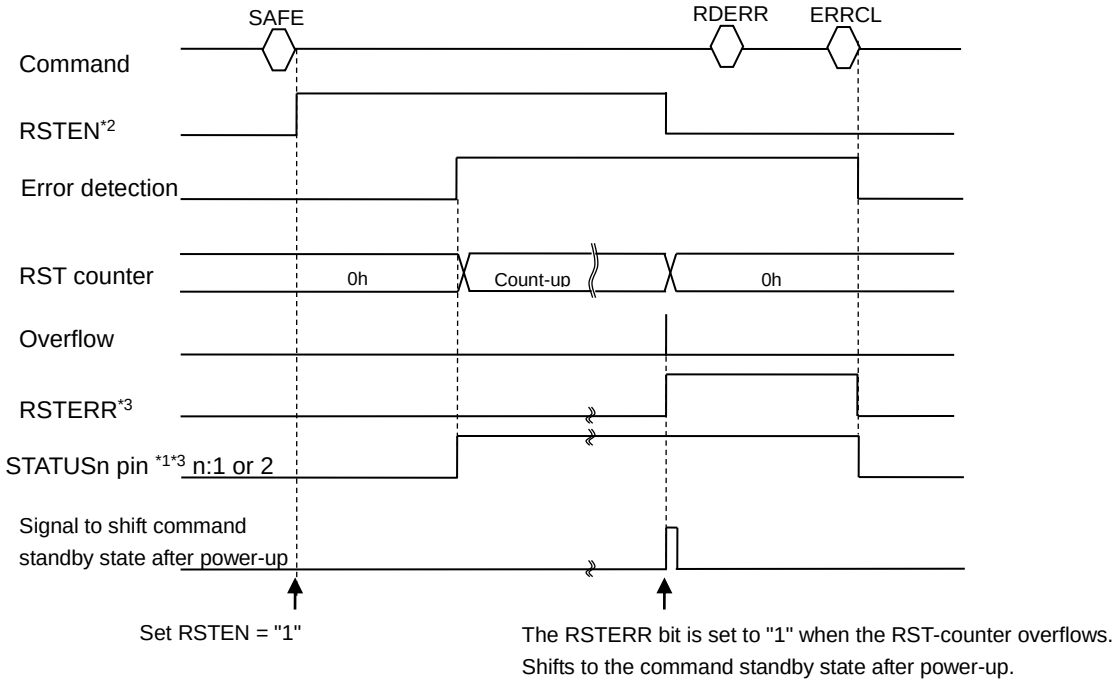
◆ RST counter overflow detection

By using the RST counter overflow detection, it is possible to shift the LSI to the command standby state after power-up after misoperation detection and failure detection occurs.
When the overflow detection of RST counter is set by RSTEN bit of SAFE command, the detection operation will start.
When the detection operation is started, the detection does not stop even if the RSTEN bit is set to "0".
The RST counter starts counting up after misoperation detection and failure detection occurs.
If the RST counter is cleared with the ERRCL command before it overflows, it stops until the next error occurs.
When the RST counter overflows, the error bit (RSTERR) is set to "1".
Error bit (RSTERR) can be read with RDERR command. Also, error bit (RSTERR) can be cleared by ERRCL command.
The count time of the RST-counter is 2s, the initial-value. The counting time can be set to 125ms, 500ms, 2s, or 4s.
Set the counting time and overflow operation (shift to the command standby state after power-up) with the dedicated tools (Speech LSI Utility).
The operation when RSTEN is set to "1" is as follows.



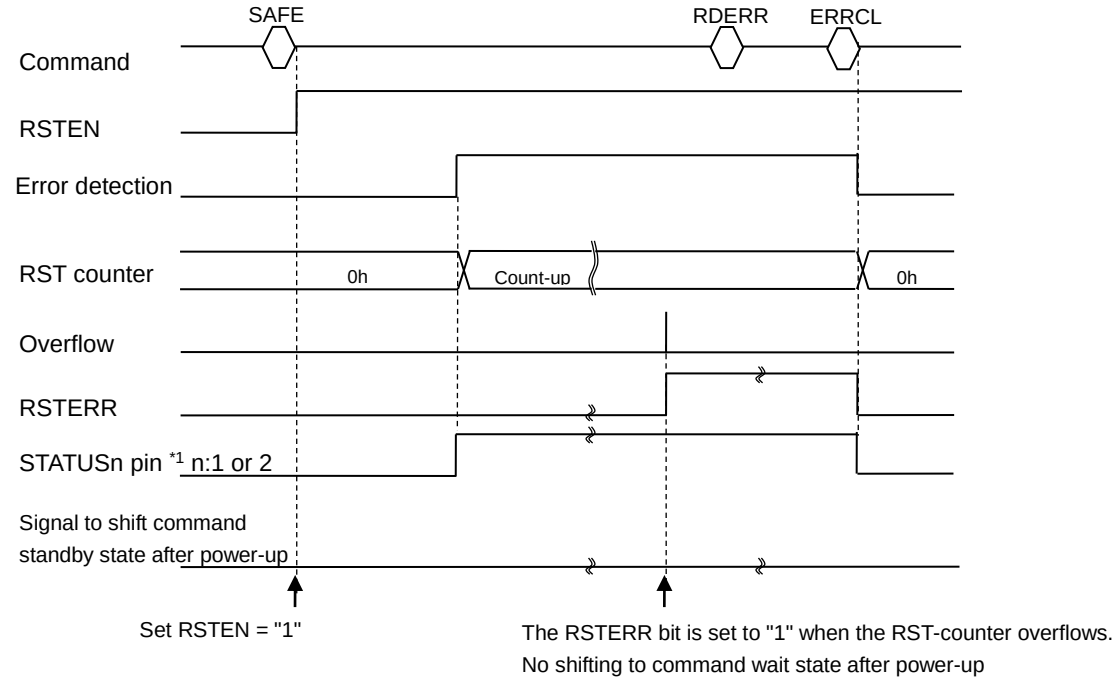
*1 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

The operation when no ERRCL command is entered is as follows.
<When "Transition to command standby state after power-up" is selected by the overflow of the RST counter>



*1 Misoperation detection and failure detection outputs are selected by OUTSTAT command.
*2 If transferring to the command standby state after power-up is executed by the overflow of the RST counter, each bit of SAFE command is cleared. Also, error bits readable by RDERR command are cleared by ERRCL command.
*3 Even if transferring to the command standby state after power-up is executed by the overflow of the RST counter, error bits readable by RDERR command and the state configured by OUTSTAT command remain.

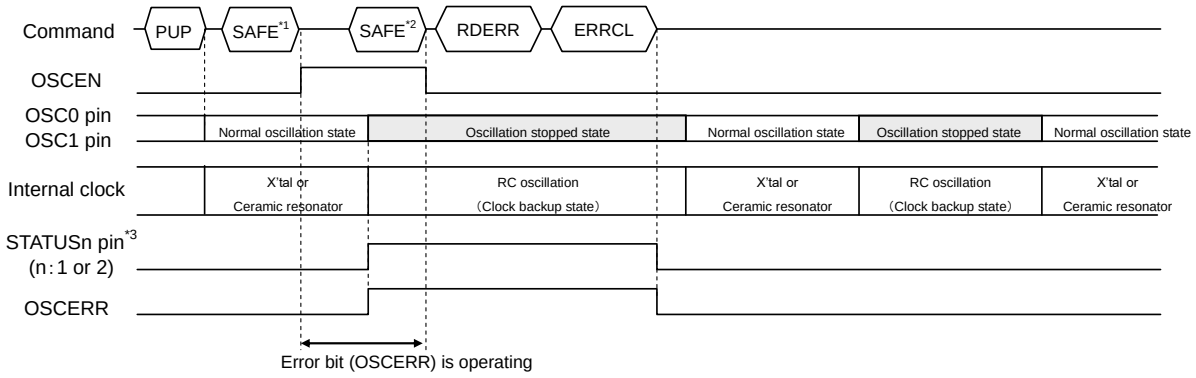
< When "Transition to command standby state after power-up " is not selected by the overflow of the RST counter >



*1 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

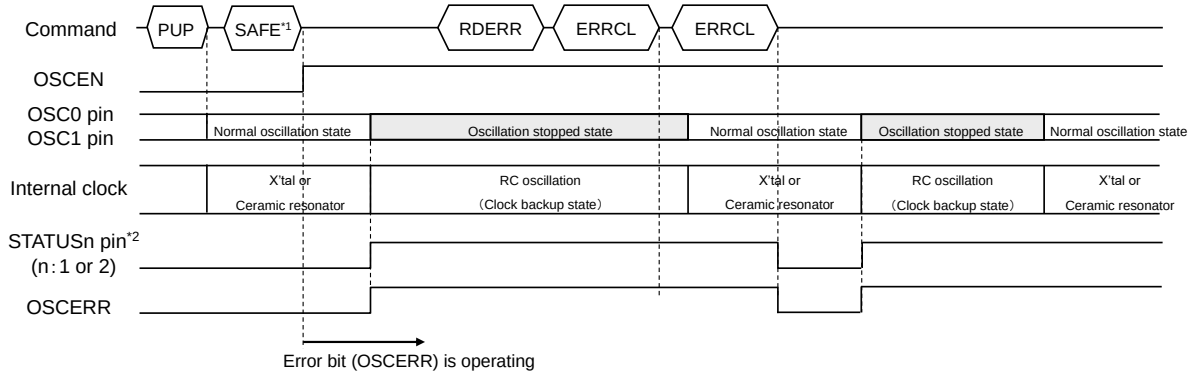
◆ Detects the stop of clock input from a crystal resonator or ceramic resonator

Set the "Detects the stop of clock input from a crystal resonator or ceramic resonator" with the OSCEN bit of the SAFE command.
When the clock input from the crystal resonator or the ceramic resonator is stopped, the error bit (OSCERR) is set to "1". At the same time, the clock backup function is activated and the clock is automatically switched to the RC oscillator circuit (4.096MHz).
Error bit (OSCERR) can be read with RDERR command. However, if the RDERR command (first byte) is inputted before the crystal or ceramic resonator stops and switches to RC oscillation (about 500us), the CBUSYB pin will remain "L". Therefore, read the command after the CBUSYB pin becomes "H". Also, error bit (OSCERR) can be cleared by ERRCL command. However, if the clock input from the crystal resonator or the ceramic resonator continues to be stopped while the OSCEN bit of the SAFE command is "1", the error bit (OSCERR) is set to "1".
When the crystal resonator or the ceramic resonator stops and switches to RC oscillation, playback may become abnormal. Therefore, after confirming that the error bit (OSCERR) is "1", enter STOP command to stop playback.
If the clock input from the crystal resonator or the ceramic resonator is stopped while the OSCEN bit is "0", the error bit (OSCERR) does not change to "1", but the clock backup function is activated and the clock backup circuit is automatically switched to the RC oscillator circuit (4.096MHz).



*1 Set OSCEN = "1"
*2 Set OSCEN = "0"
*3 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

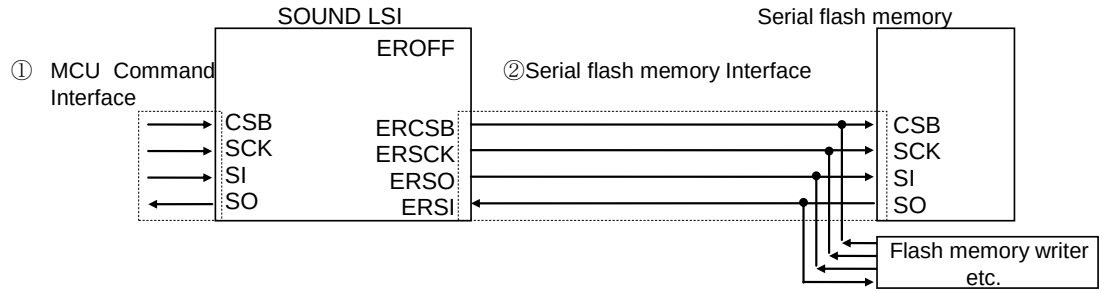
<When the OSCEN bit of SAFE command continue to be "1">



*1 Set OSCEN = "1"
*2 Misoperation detection and failure detection outputs are selected by OUTSTAT command.

- Serial flash memory rewrite function

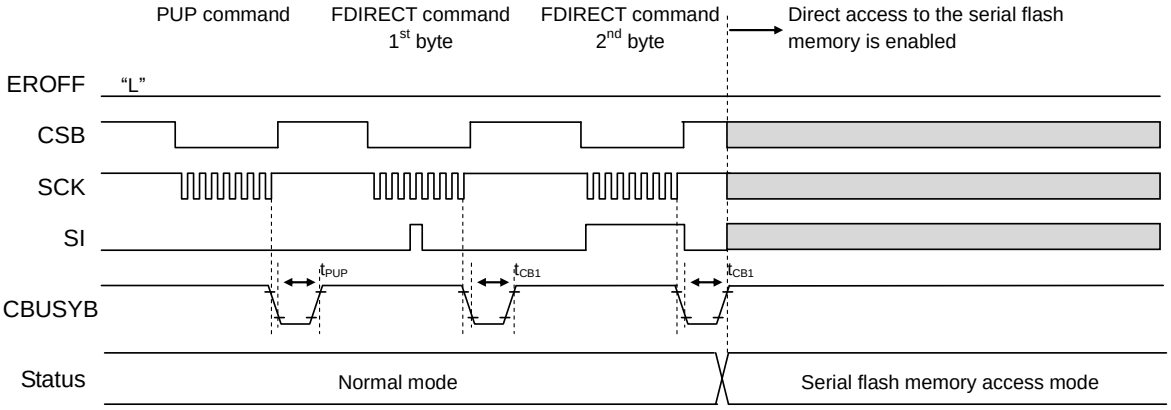
The serial flash memory can be rewritten in the following two ways.



① Rewrite using the clock synchronous serial interface of the MCU command interface

By using the CSB, SCK, SI and SO pins, which are clock synchronous serial interfaces of the MCU command interface the serial flash memory can be rewritten. When the PUP command and FDIRECT command are entered with the EROFF pin set to "L", direct access to the serial flash memory is enabled from the CSB, SCK, SI and SO pins. At that time, set the SCK pin to 'H' level when the CSB pin falls, and data should be taken in on the rising edge of the SCK pin clock and output data on the falling edge.

When returning to the normal mode, insert a reset to initialize (RESETB pin is “L” level.) or shut off the power.

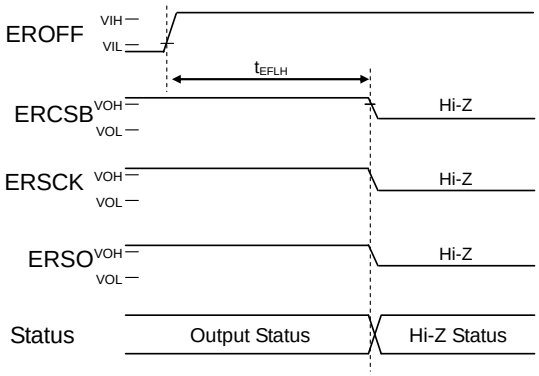


For the PUP command, refer to the "PUP command" in the "Command" section. For the FDIRECT command, refer to the "FDIRECT command" in the "Command" section.

② Rewrite using serial flash memory interface without this LSI

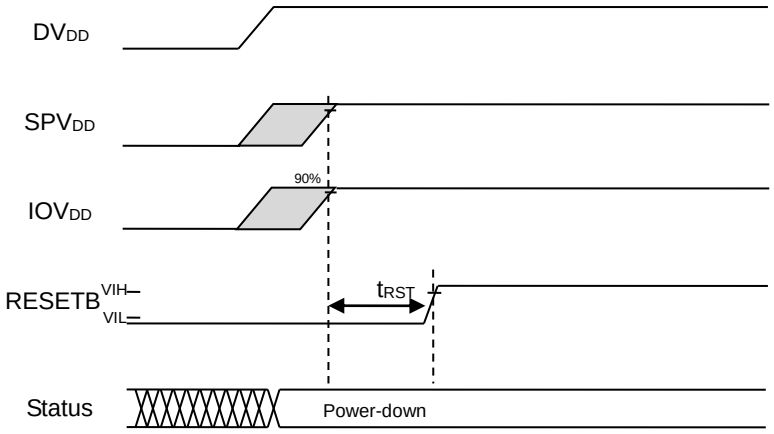
The serial flash memory can be rewritten using the ERCSB, ERSCK, ERSI and ERSO pins that is the serial flash memory interface.

When the EROFF pin set to "H", the serial flash memory can be rewritten using the ERCSB, ERSCK, ERSI and ERSO pins without this LSI. (ERCSB, ERSCK and ERSO pins are in a condition of high-impedance.)



■ Timing chart

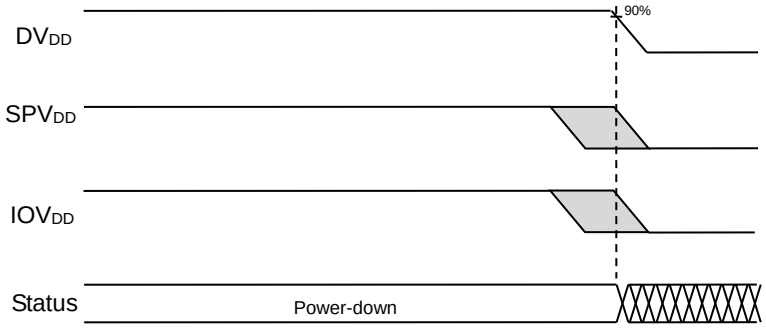
- Power-on timing



After the power is turned on, the device enters the power-down state.
Start up in order of DV_{DD}, SPV_{DD} and IOV_{DD} or DV_{DD}, IOV_{DD} and SPV_{DD}.
It is possible that the DV_{DD} and SPV_{DD} start up at the same time and then the IOV_{DD} starts up, or the DV_{DD} and IOV_{DD} start up at the same time and then the SPV_{DD} starts up.
The DV_{DD}, SPV_{DD} and IOV_{DD} can also start up at the same time.
t_{RST} is specified based on the last power-on pin.

Be sure to input "L" to the RESETB pin before inputting the first command after power-on.
Be sure to enter "L" at the RESETB pin when the DV_{DD} is below the (recommended) operating voltage range.

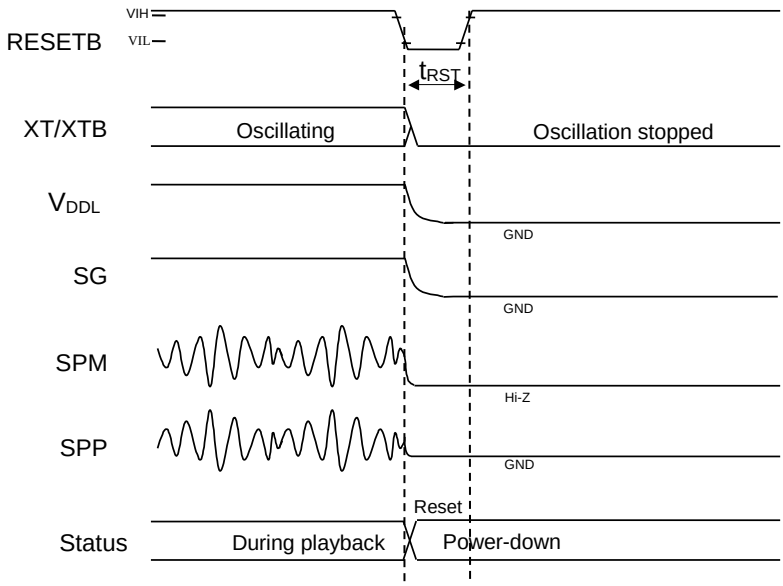
- Power-off timing



Shut down in order of IOV_{DD}, SPV_{DD}, and DV_{DD} or SPV_{DD}, IOV_{DD}, and DV_{DD}.
It is possible that the IOV_{DD} shuts down and then the SPV_{DD} and DV_{DD} shut down at the same time, or the SPV_{DD} shuts down and then the IOV_{DD} and DV_{DD} shut down at the same time.
The DV_{DD}, SPV_{DD} and IOV_{DD} can also shut down at the same time.

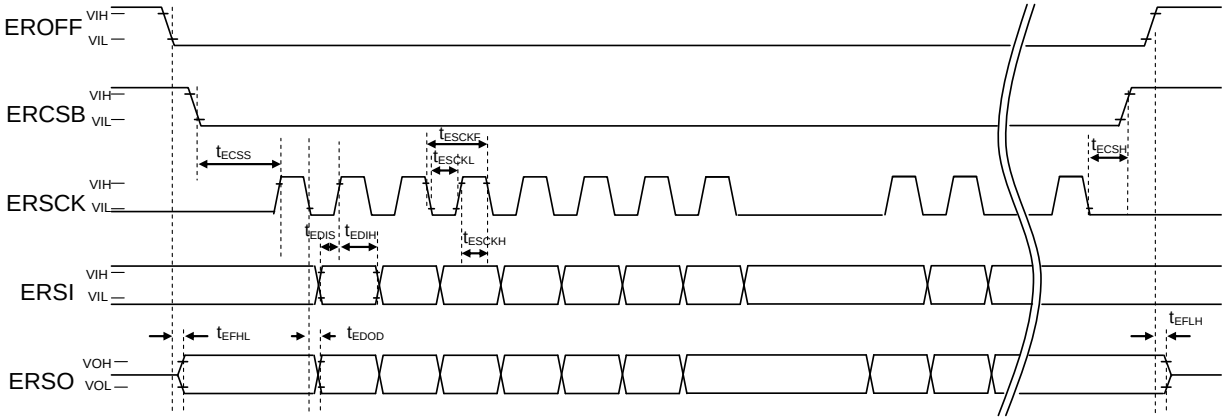
Shut down each power supply after changing to the power down status with PDWN commands.

- Reset input timing



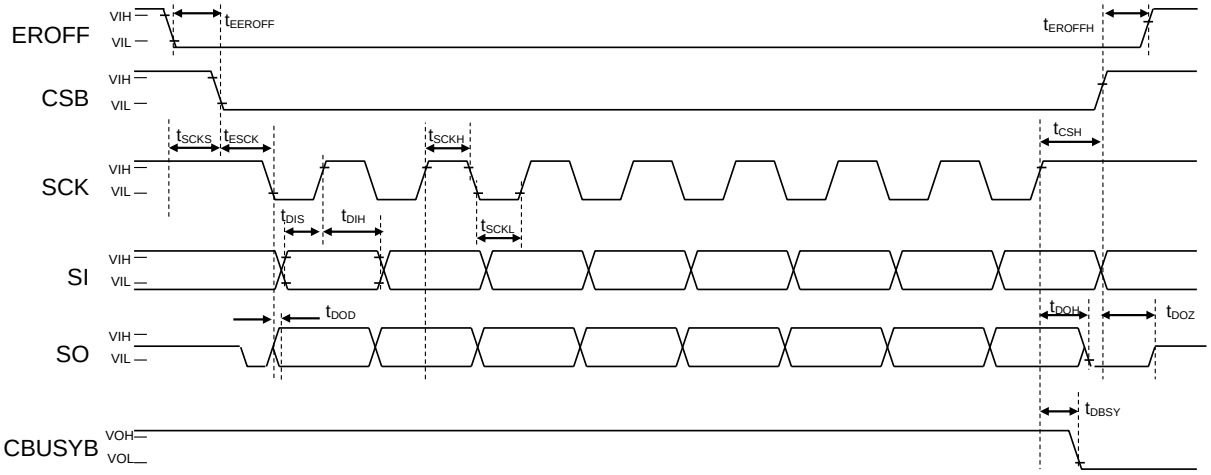
The same timing is applied when a reset is input during command standby.

- Serial flash memory interface timing

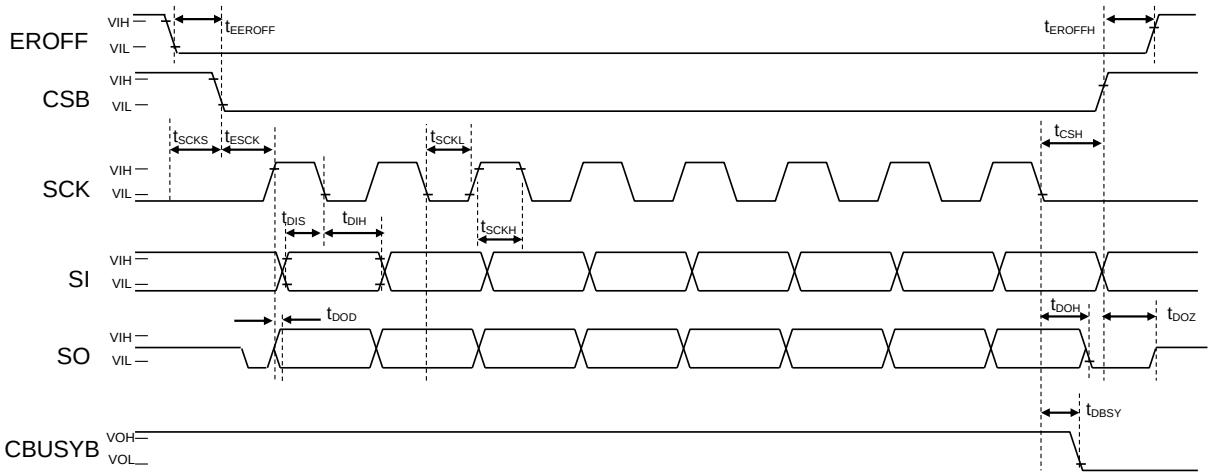


- Clock synchronous serial

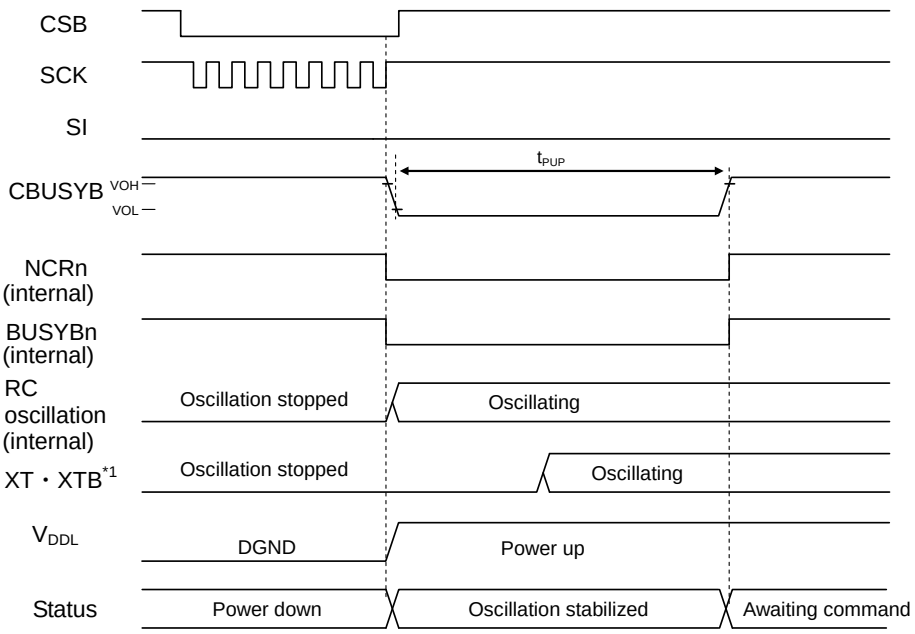
◆ Clock Synchronous Serial Interface Timing (SCK Initial Value = "H" Level)



◆ Clock Synchronous Serial Interface Timing (SCK Initial Value = "L" Level)

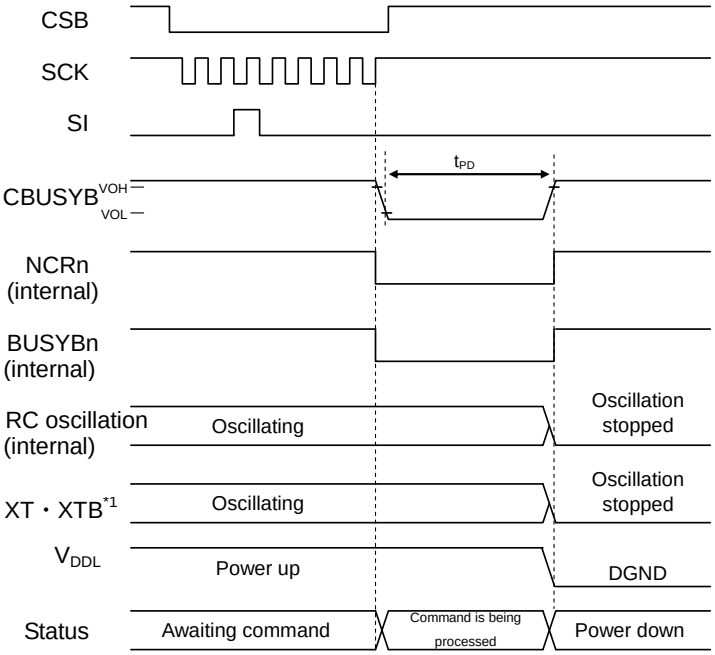


- Power-up timing



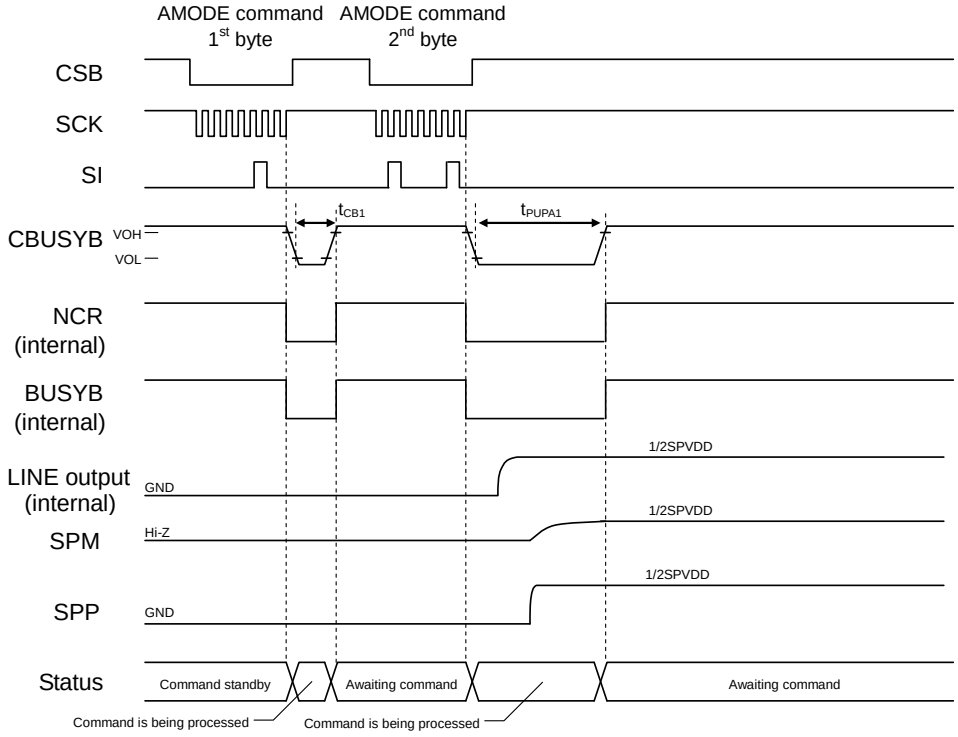
*1 When using a crystal or ceramic resonator

- Power-down timing

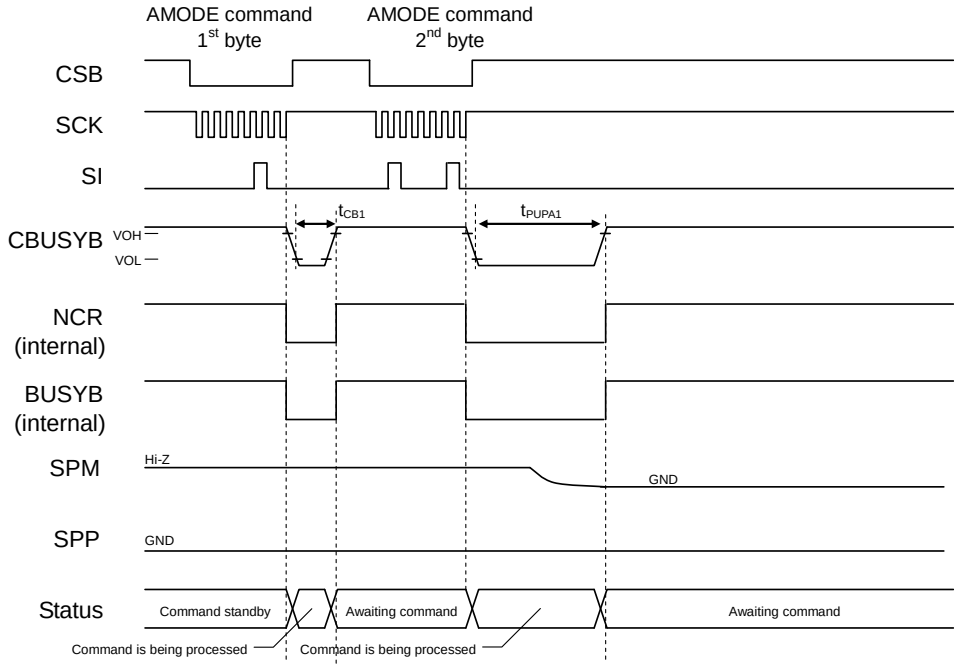


*1 When using a crystal or ceramic resonator

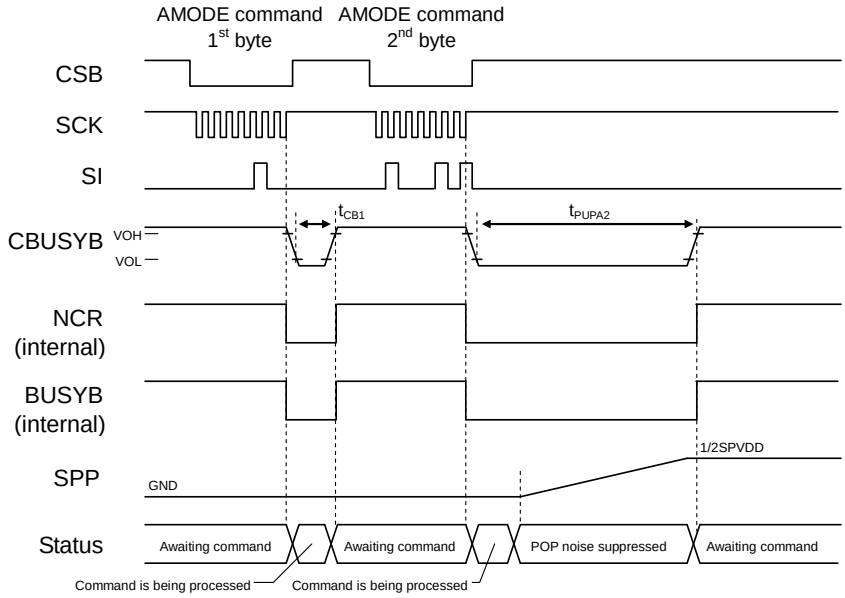
- Speaker amplifier power-up timing (DAMP bit = "0", AEN1 bit = "0", AEN0 bit = "0" → "1")



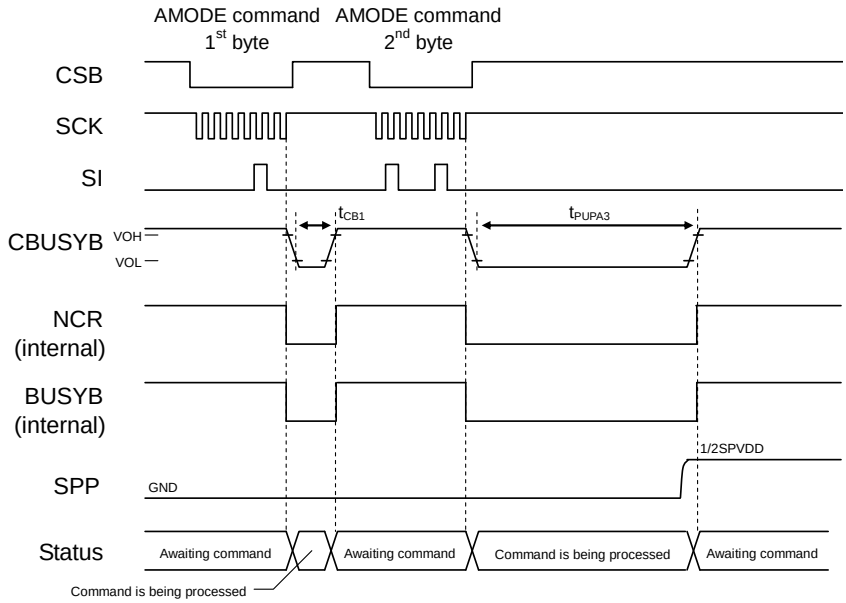
- Speaker amplifier power-up timing (DAMP bit = "1", AEN1 bit = "0", AEN0 bit = "0" → "1")



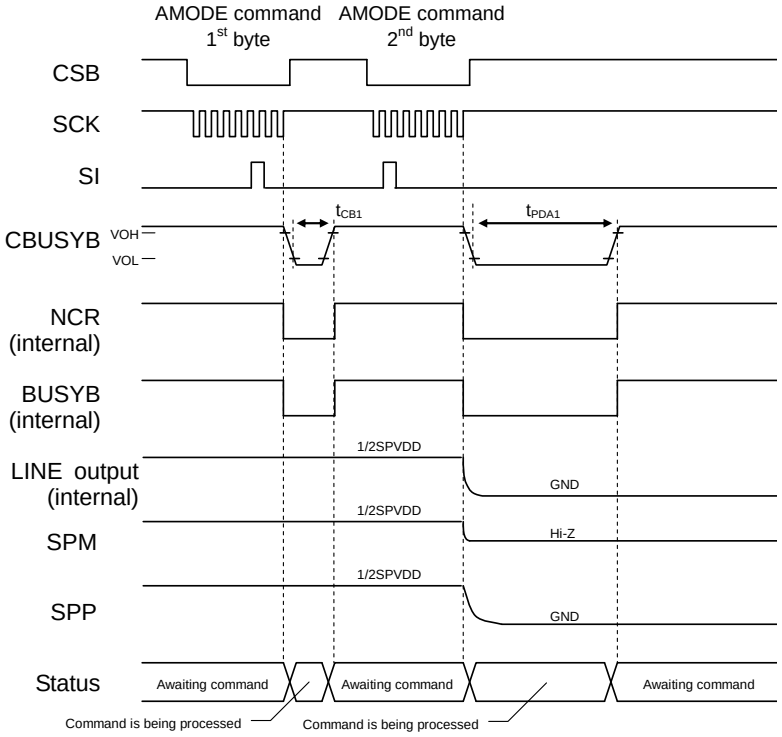
- Line amplifier power-up timing (DAMP bit = "0", POP bit = "1", AEN1 bit = "0" → "1", AEN0 bit = "0")



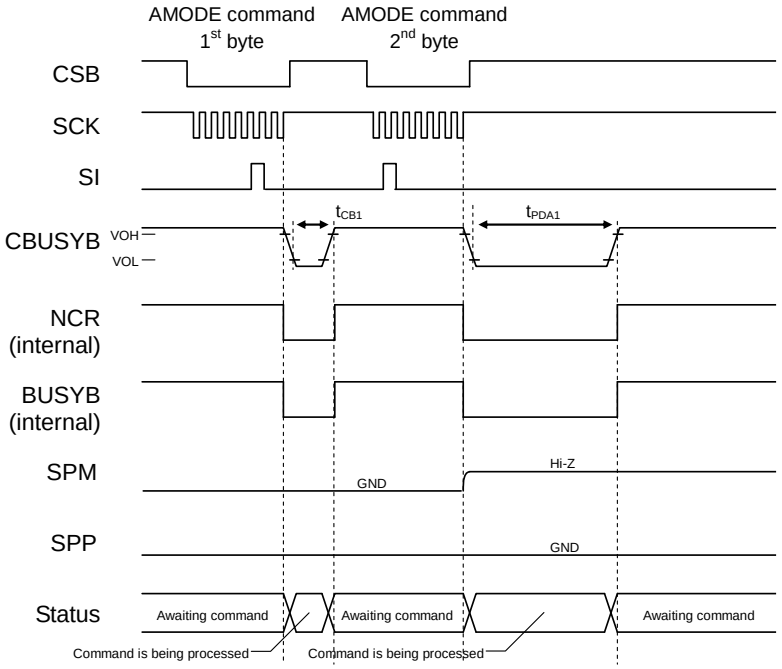
- Line amplifier power-up timing (DAMP bit = "0", POP bit = "0", AEN1 bit = "0" → "1", AEN0 bit = "0")



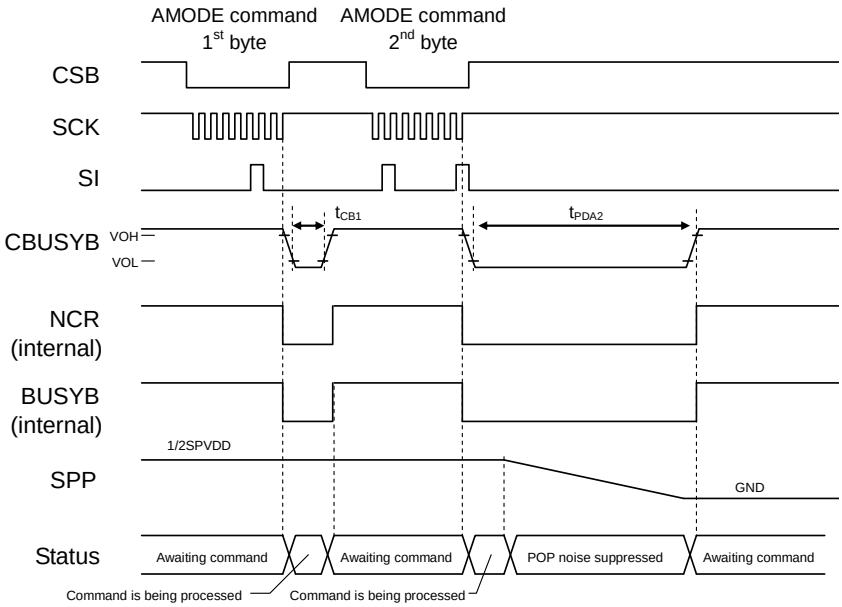
- Speaker amplifier power-down timing (DAMP bit = "0", AEN1 bit = "0", AEN0 bit = "1" → "0")



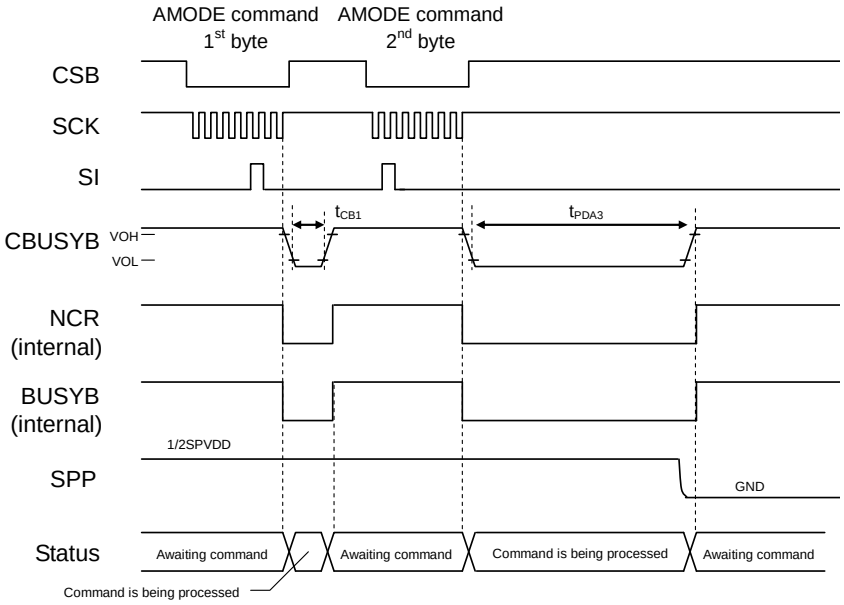
- Speaker amplifier power-down timing (DAMP bit = "1", AEN1 bit = "0", AEN0 bit = "1" → "0")



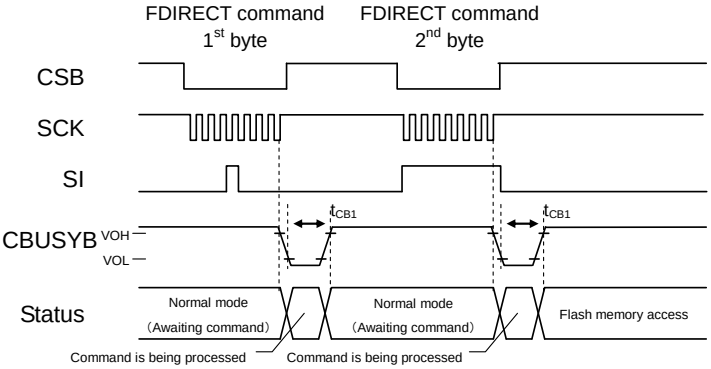
- Line amplifier power-down timing (DAMP bit = "0", POP bit = "1", AEN1 bit = "1" → "0", AEN0 bit = "0")



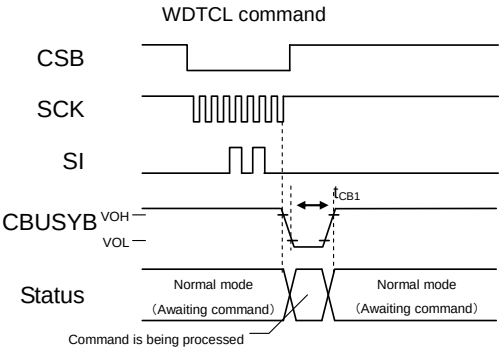
- Line amplifier power-down timing (DAMP bit = "0", POP bit = "0", AEN1 bit = "1" → "0", AEN0 bit = "0")



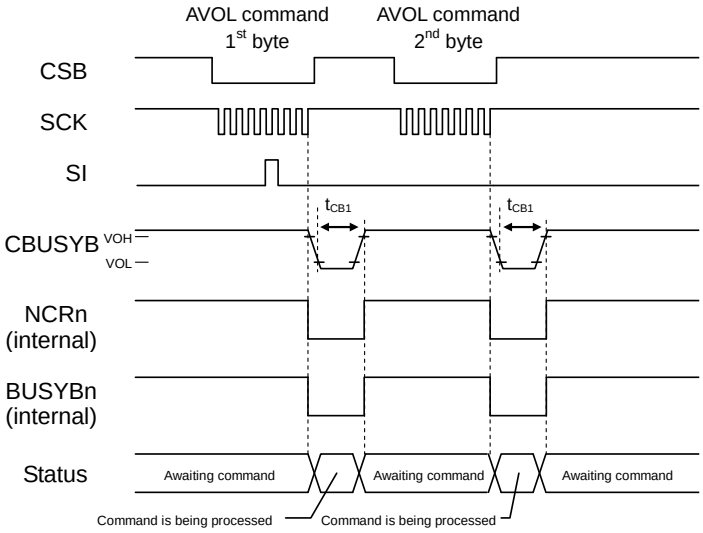
- FDIRECT command timing



- WDTCL command timing

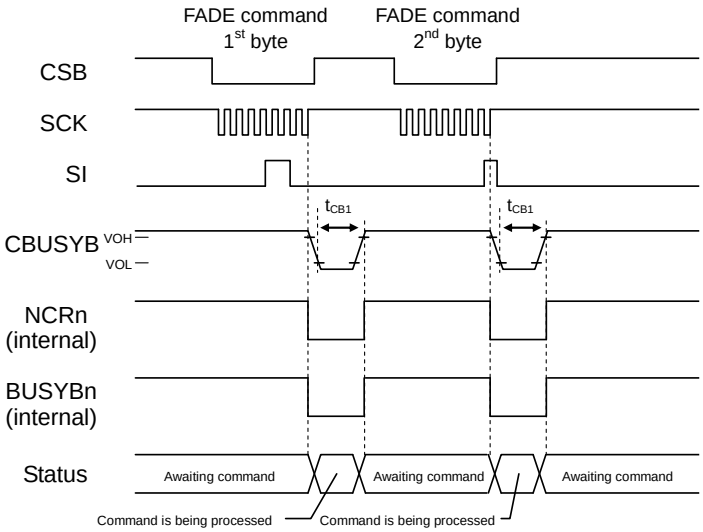


- Change volume timing by AVOL command

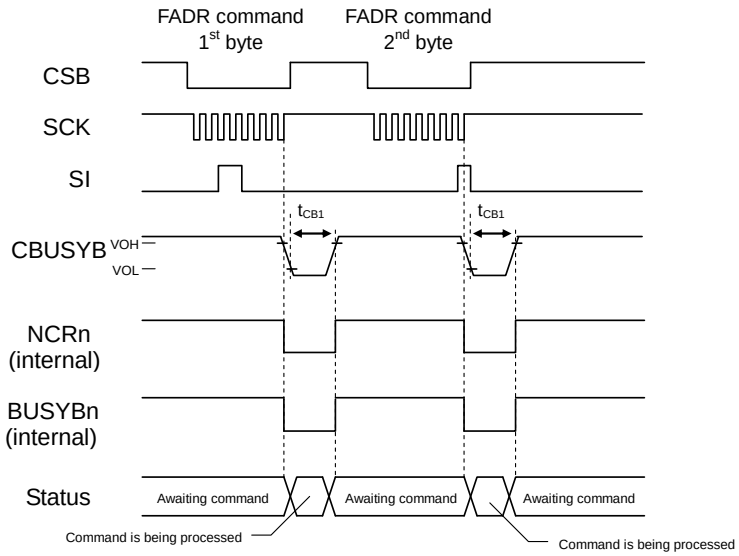


Speaker amplifier volume setting by AVOL commands is valid only when Class AB speaker amplifier is used.
When a Class D speaker amplifier is used, the setting value is ignored and +0.0dB is selected.

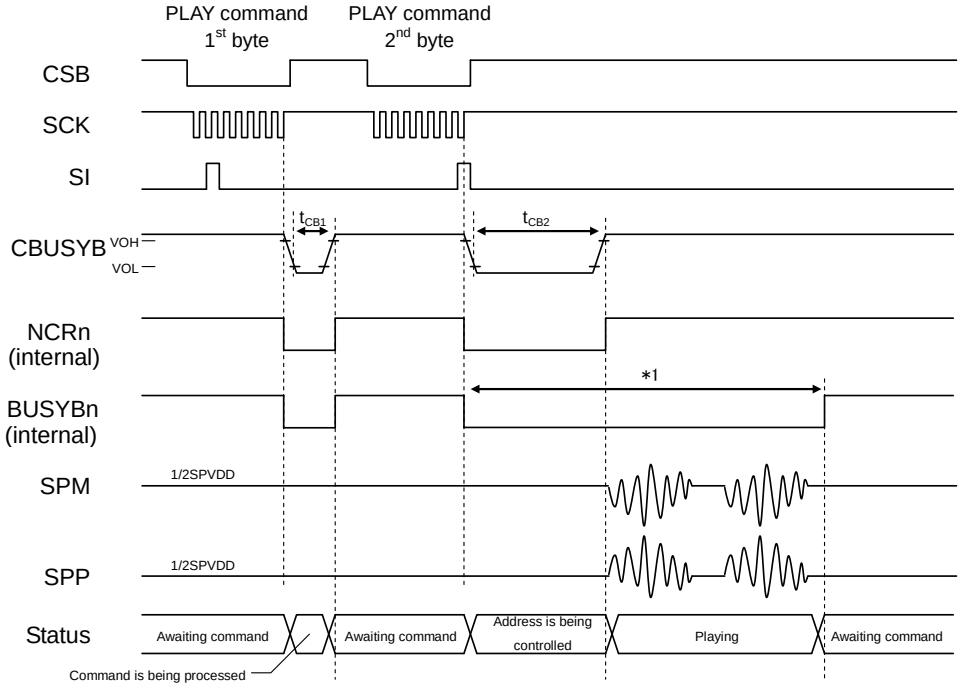
- FADE command timing



- Setting playback phrases using FADR command



- Playback start timing by PLAY command

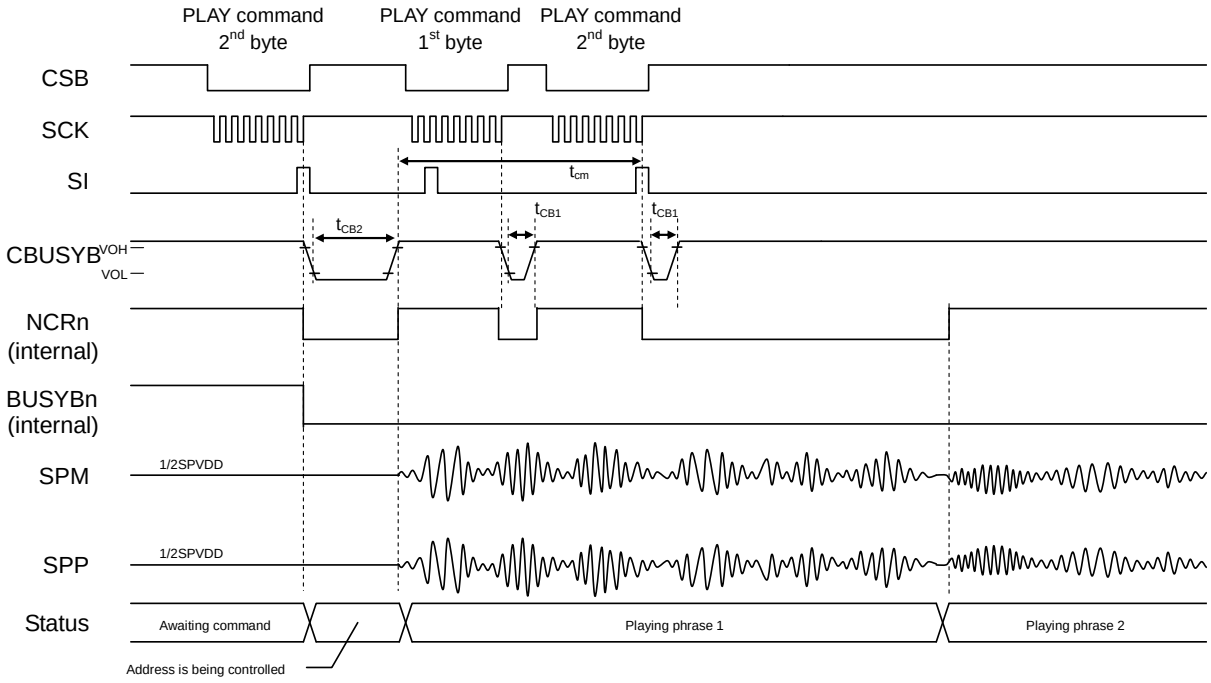


When the first byte of the PLAY command is input, the device waits for the input of the second byte after the command processing time (t_{CB1}). When the second byte is entered, the address data of the phrase to be played after the command processing time (t_{CB2}) is read from the flash memory.
When the phrase address data is read, the specified phrase starts playback, and when playback is completed, the BUSYB signal of the playback channel becomes "H" level.

The NCR signal goes to the "L" level during playback preparation, and goes to the "H" level when playback preparation is completed and playback starts. When the NCR signal of the playback channel becomes "H" level, the PLAY command of the next phrase to be played can be accepted.

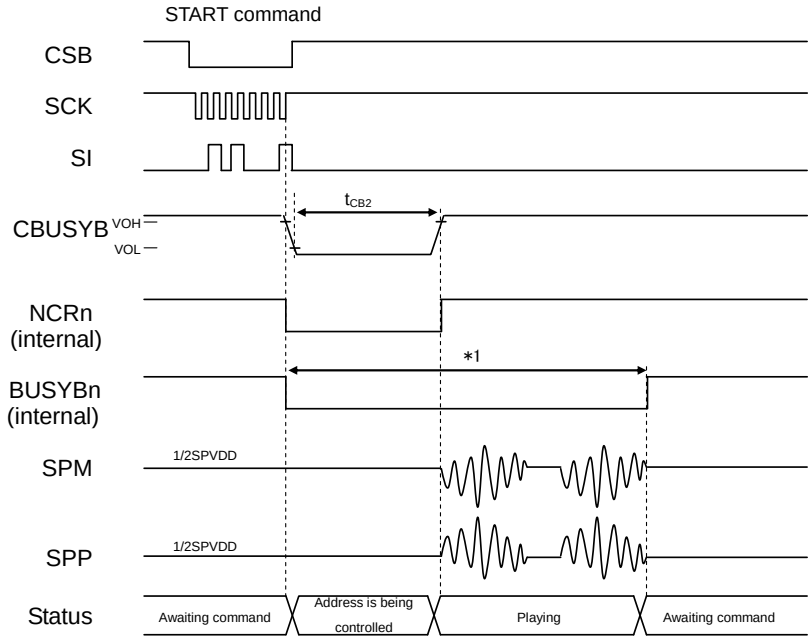
*1 The length of the "L" interval in the BUSYBn is (tCB2+ sound production time).

- Continuous playback timing by PLAY command



When making continuous playbacks, input the PLAY command for the next phrases within the specified time period (tcm) after the NCR of the corresponding channel changes to "H" level, so that the LSI plays back the next phrases without silence sounds after the current phrase playback ends.
When the playback is not continuous, input the PLAY command for the next phrases after confirming the playback is completed by RDSTAT command, etc.

- Playback start timing by START command

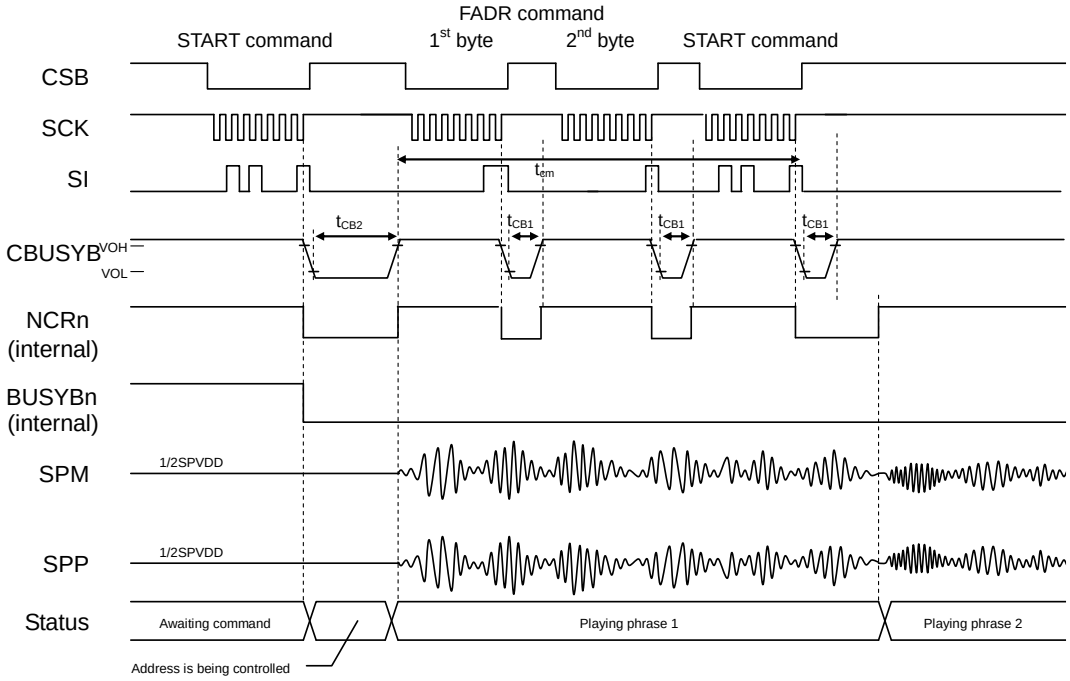


When the START command is input, the address data of the phrase to be played after the command processing time (t_{CB2}) is read from the flash memory. When the phrase address data is read, the specified phrase starts playback, and when playback is completed, the BUSYB signal of the playback channel becomes "H" level.

The NCR signal goes to the "L" level during playback preparation, and goes to the "H" level when playback preparation is completed and playback starts. When the NCR signal of the playback channel becomes "H" level, the START command of the next phrase to be played can be accepted.

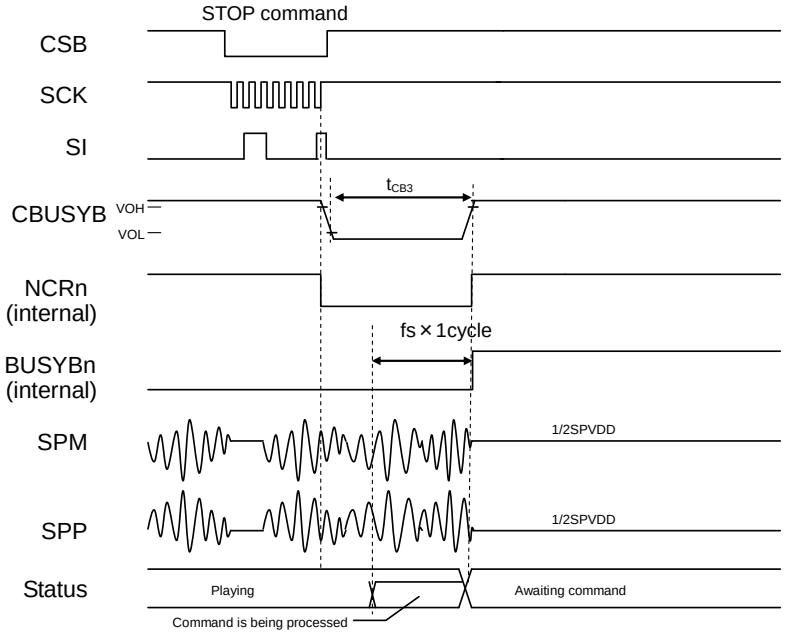
*1 The length of the "L" interval in the BUSYBn is (tCB2+ sound production time).

- Continuous playback timing by START command

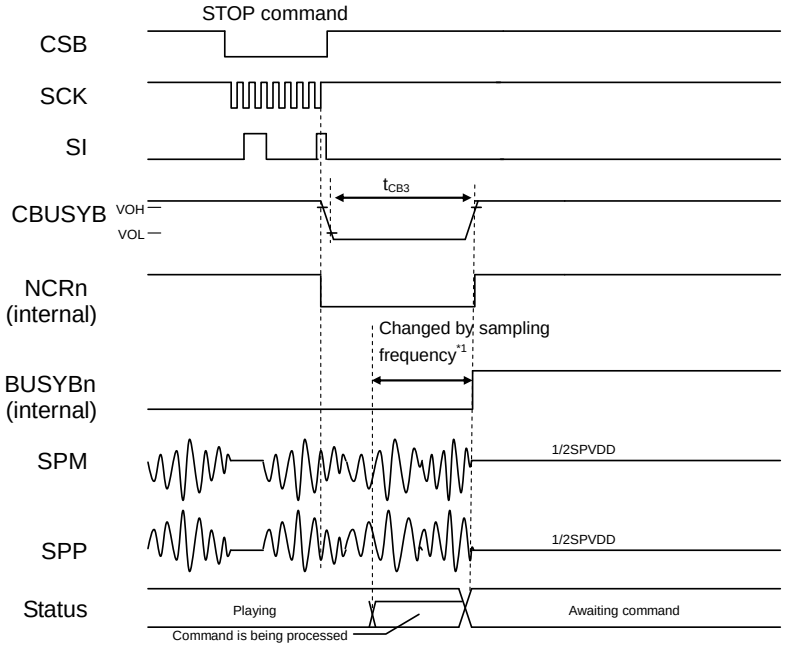


When making continuous playbacks, input the START command for the next phrases within the specified time period (tcm) after the NCR of the corresponding channel changes to "H" level, so that the LSI plays back the next phrases without silence sounds after the current phrase playback ends.
When the playback is not continuous, input the START command for the next phrases after confirming the playback is completed by RDSTAT command, etc.

- STOP command (when the FAD bit is "L")



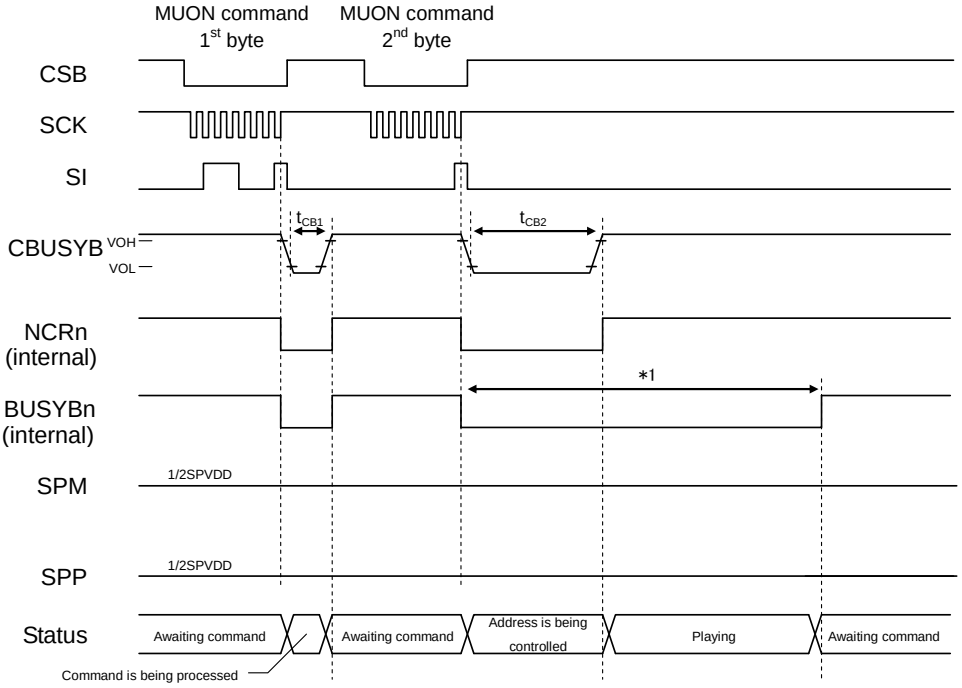
- STOP command (when the FAD bit is "H")



*1 The duration of the BUSYBn varies depending on the sampling frequency groups.

At 10.7/21.3kHz	: Approx. 3ms
At 6.4/12.8/25.6kHz	: Approx. 5ms
At 8.0/16.0/32.0kHz	: Approx. 4ms
At 11.025/22.05/44.1kHz	: Approx. 2.9ms
At 12.0/24.0/48.0kHz	: Approx. 2.7ms

- Playback start timing by MUON command

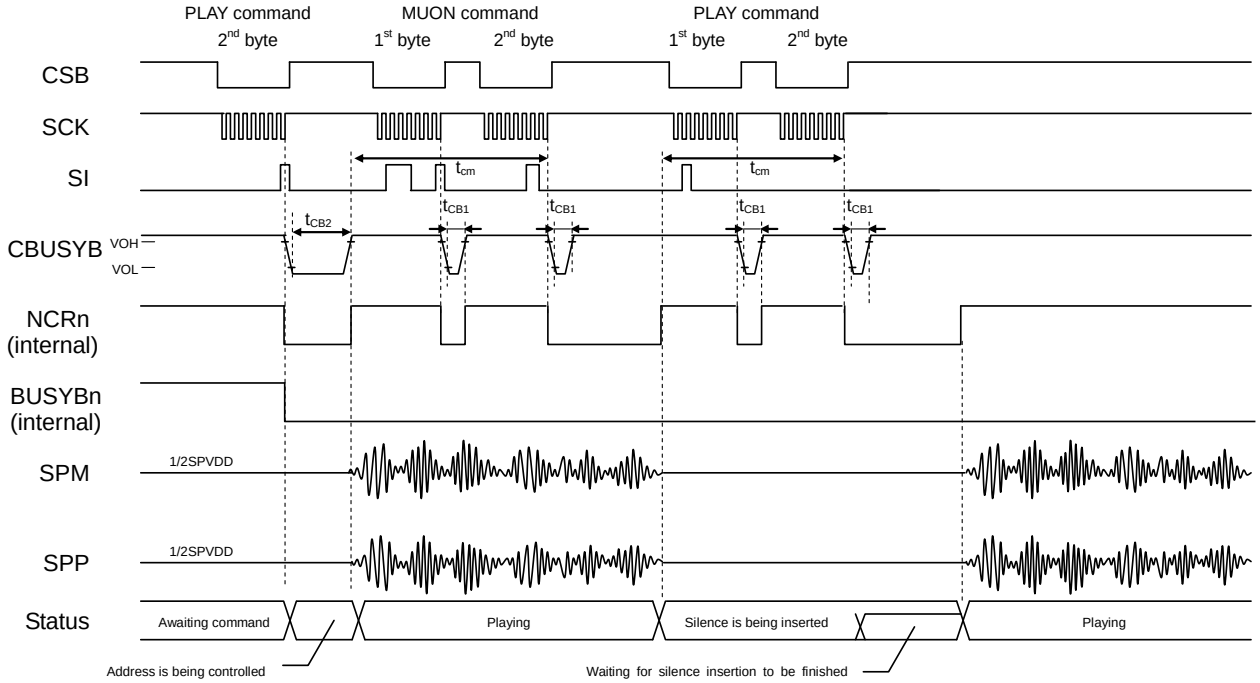


When the first byte of the MUON command is input, the device waits for the input of the second byte after the command processing time (t_{CB1}). When the second byte is entered, the silence time is calculated after the command processing time (t_{CB2}). When the calculation of the silence duration is completed, the calculated silence is played back, and when the playback is completed, the BUSYB signals of the playback channels become "H" level.

The NCR signal becomes "L" level during playback preparation, and becomes "H" level when playback preparation is completed and playback starts. When the NCR signal of the playback channel becomes "H" level, the PLAY command of the next phrase to be played can be accepted.

*1 The length of the "L" interval of the BUSYBn is (tCB2+ silence playback time).

- Continuous playback timing by MUON command



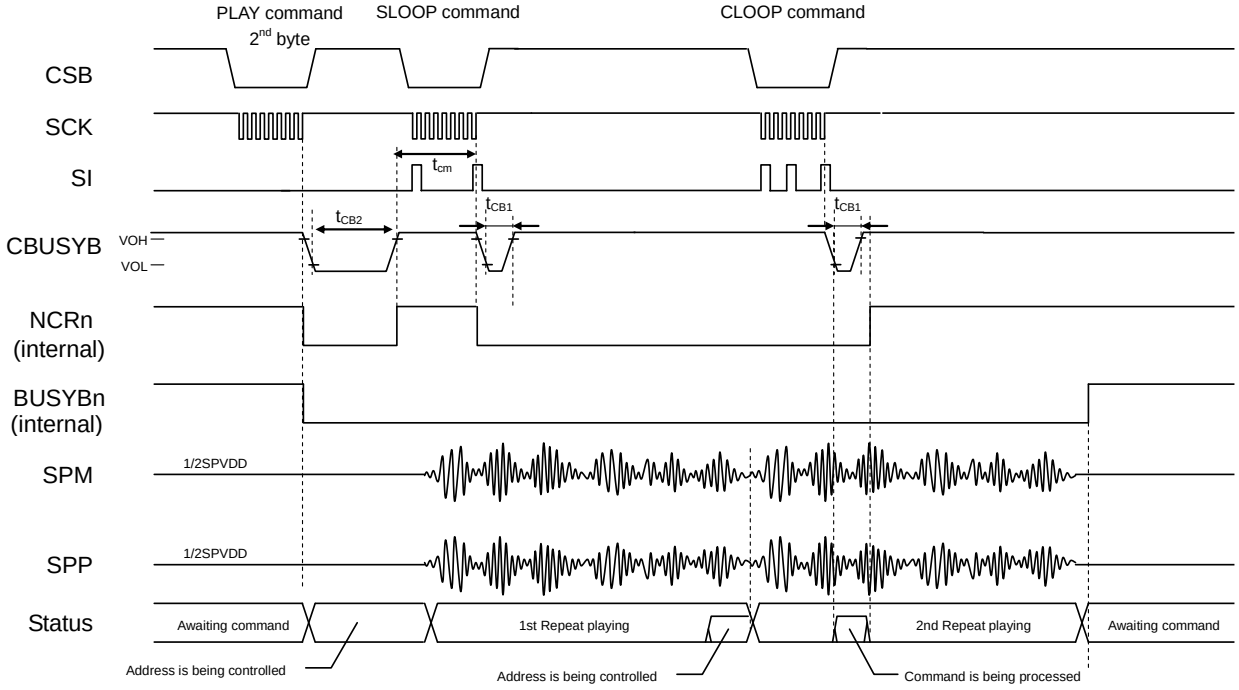
After the PLAY command is input, the CBUSYB signal and NCR signal change to "H" level when the address management of phrase 1 is completed and start playing back. Input the MUON command after the CBUSYB signal changed to "H" level. After the MUON command is received, the LSI is in a state waiting for the end of playback of phrase 1 and the NCR signal remains "L" level until the end of playback.

When the playback of phrase 1 ends, playback of the silence sound starts and the NCR signal changes to "H" level. After the NCR signal of the corresponding channel changes to "H" level, send the PLAY command again to playback the phrase 1. The NCR signal changes to "L" level again after the PLAY command is received and the LSI is in a state waiting for the end of the playback of silence sound.

After ending the playback of silence sound and starting the playback of phrase 1, the NCR signal changes to "H" level and LSI is in state that accepts the next PLAY or MUON command.
The BUSYB signal remains "L" level until the sequence of playback is completed.

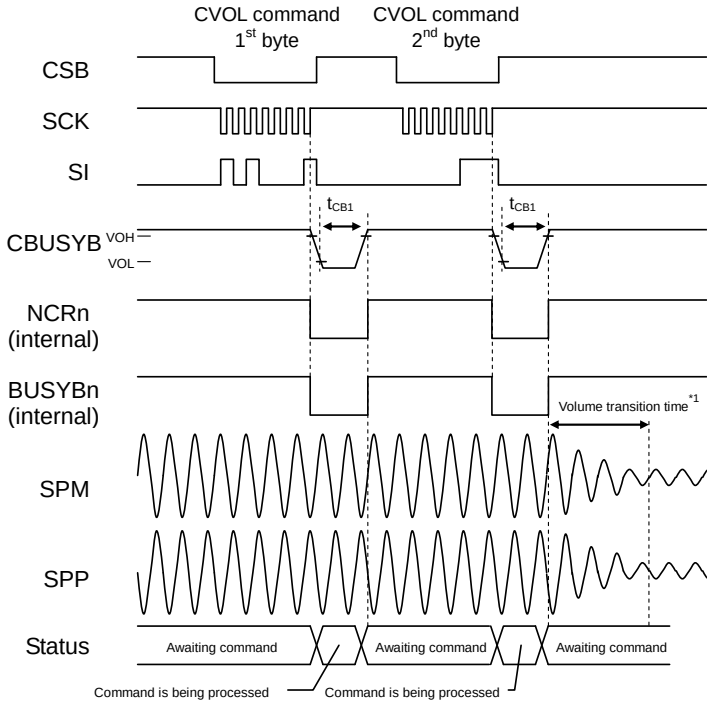
When making continuous playbacks, input the MUON/PLAY/START command for the next phrases within 10ms (tcm) after the NCR of the corresponding channel changes to "H" level.
When the playback is not continuous, input the MUON/PLAY/START command for the next phrases after confirming the playback is completed by RDSTAT command, etc.

- Repeat playback setting/release timing by SLOOP/CLOOP command



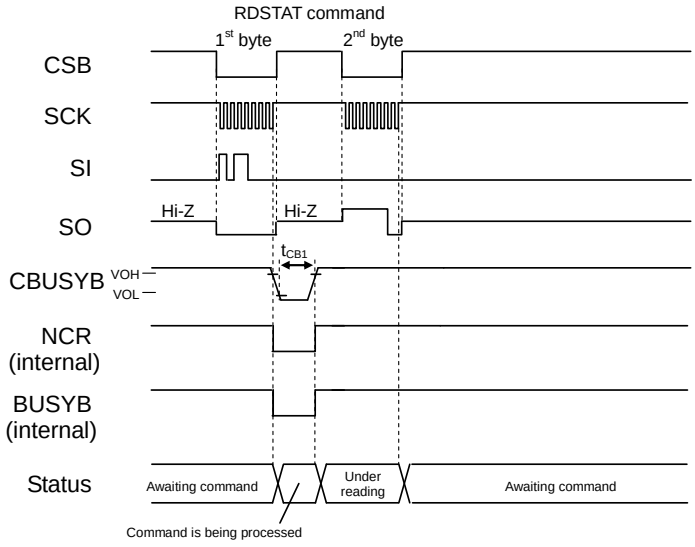
The SLOOP command is valid only during playback. After the PLAY command is input, input the SLOOP command within the specified period (t_{cm}) after the NCR of the corresponding channel becomes "H" level. This enables the SLOOP command and repeats playback. While the repeat playback mode is set, the NCR signal is "L" level.

- Change volume timing by CVOL command

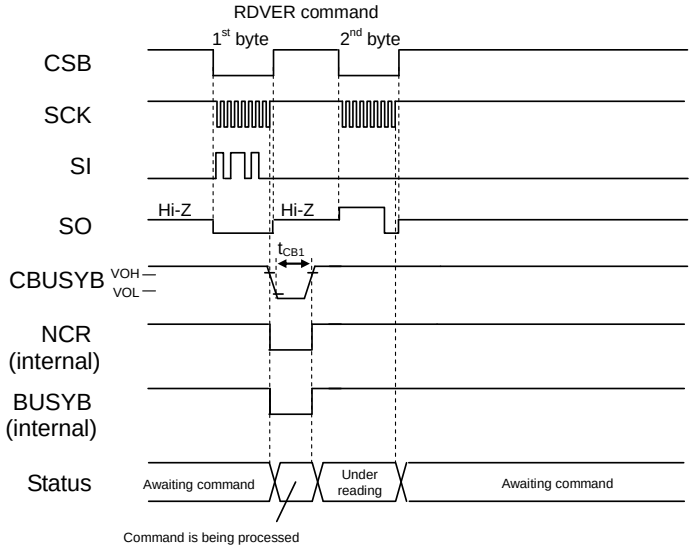


*1 Refer to the "FADE command" for more information on volume-transition time.

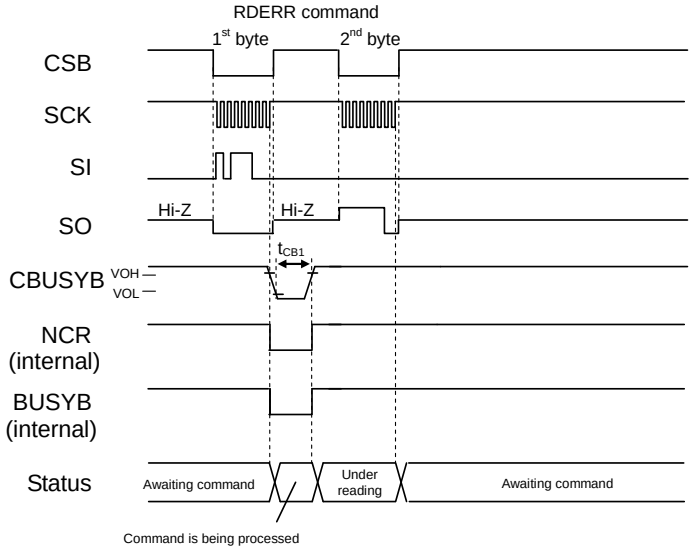
- RDSTAT command timing



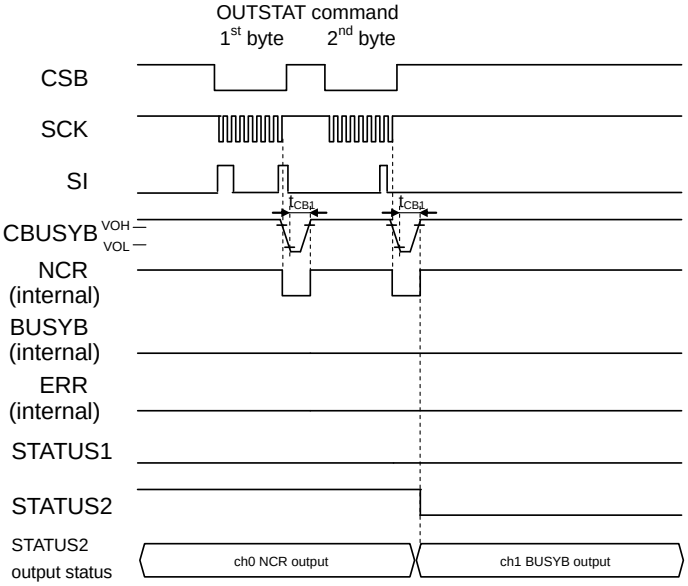
- RDVER command timing



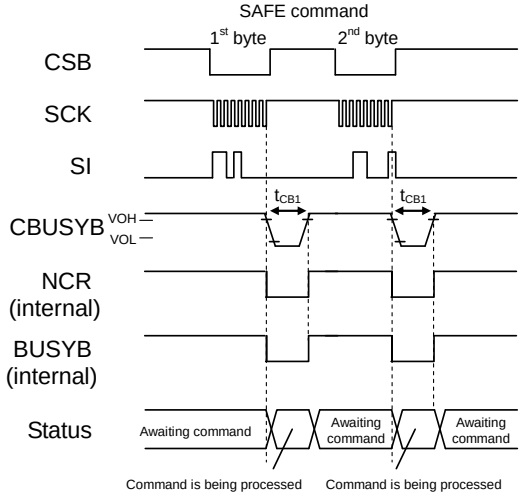
- RDERR command timing



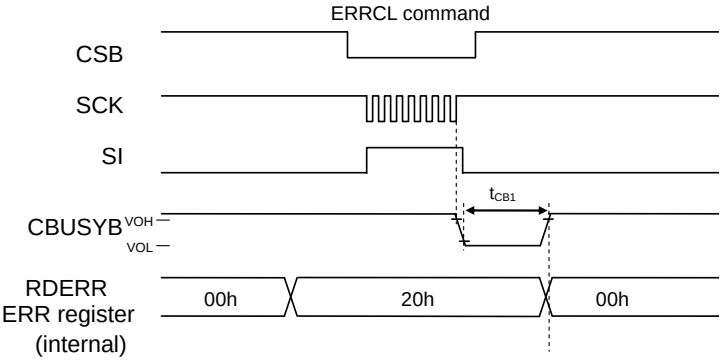
- OUTSTAT command timing



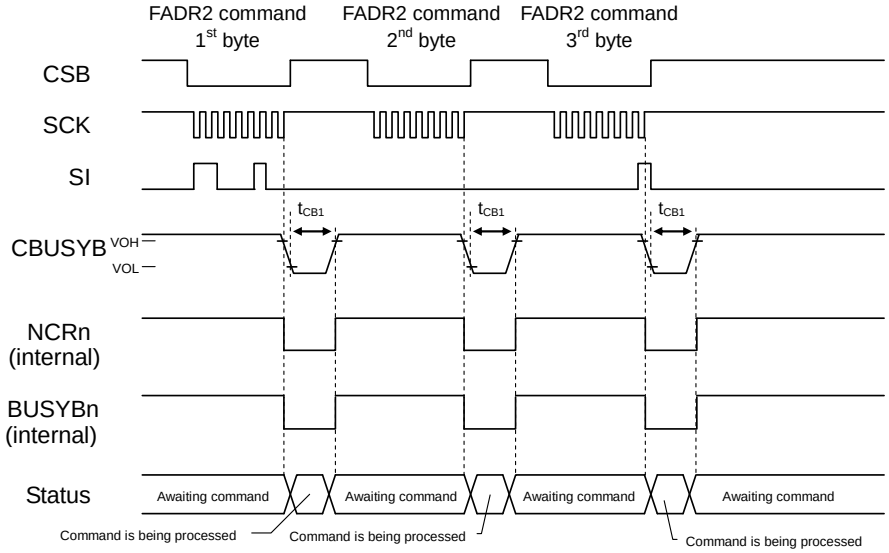
- SAFE command timing



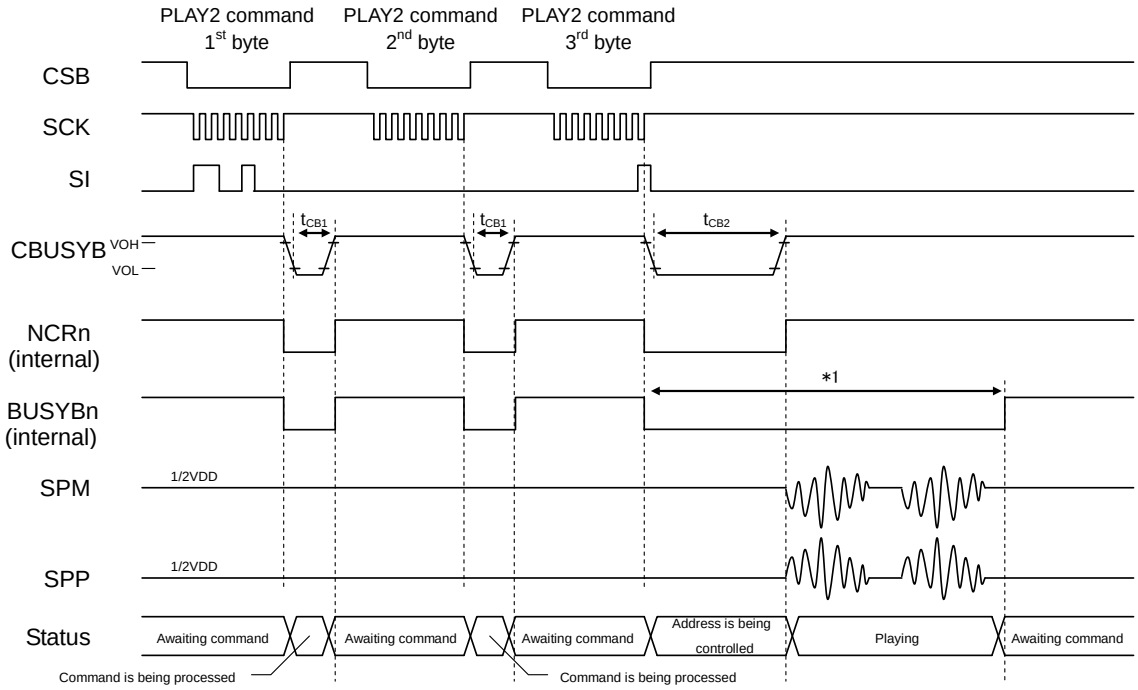
- ERRCL command timing



- Setting timing of playback phrases by FADR2 command



- Playback start timing by PLAY2 command



When the first byte of the PLAY command is input, the 2nd byte waits for input after the command processing time (t_{CB1}), and when the 2nd byte is input, the 3rd byte waits for input after the command processing time (t_{CB1}). When the third byte is entered, the address data of the phrase to be played after the command processing time (t_{CB2}) is read from the flash memory. When the phrase address data is read, the specified phrase is played back, and when playback is completed, the BUSYB signal of the playback channel becomes "H" level.

The NCR signal goes to the "L" level during playback preparation, and goes to the "H" level when playback preparation is completed and playback starts. When the NCR signal of the playback channel becomes "H" level, the PLAY command of the next phrase to be played can be accepted.

*1 The length of the "L" interval in the BUSYBn is (tCB2+ sound production time).

■ Command

- Command list

Each command is configured in 1-byte (8-bit) units. The PUP, WDTCL, PDWN, START, STOP, SLOOP, CLOOP and ERRCL commands are configured by one byte, the FADR2 and PLAY2 command are configured by three bytes, and the other commands are configured by two bytes.
Do not enter command that is not described in this manual. Enter the command with the CBUSYB "H".

Command name	D7	D6	D5	D4	D3	D2	D1	D0
PUP	0	0	0	0	0	0	0	WCM
AMODE	0	0	0	0	0	1	DAMP	HPF
	FAD	DAG1	DAG0	AIG1	AIG0	AEN1	AEN0	POP
AVOL	0	0	0	0	1	0	0	0
	0	0	AV5	AV4	AV3	AV2	0	0
FADE	0	0	0	0	1	1	0	0
	0	0	0	0	FCON2	FCON1	FCON0	FADE
FDIRECT	0	0	0	1	0	0	0	0
	PRT7	PRT6	PRT5	PRT4	PRT3	PRT2	PRT1	PRT0
WDTCL	0	0	0	1	0	1	0	0
PDWN	0	0	1	0	0	0	0	0
FADR	0	0	1	1	F9	F8	C1	C0
	F7	F6	F5	F4	F3	F2	F1	F0
PLAY	0	1	0	0	F9	F8	C1	C0
	F7	F6	F5	F4	F3	F2	F1	F0
START	0	1	0	1	CH3	CH2	CH1	CH0
STOP	0	1	1	0	CH3	CH2	CH1	CH0
MUON	0	1	1	1	CH3	CH2	CH1	CH0
	M7	M6	M5	M4	M3	M2	M1	M0
SLOOP	1	0	0	0	CH3	CH2	CH1	CH0
CLOOP	1	0	0	1	CH3	CH2	CH1	CH0
CVOL	1	0	1	0	CH3	CH2	CH1	CH0
	0	CV1	CV0	CV6	CV5	CV4	CV3	CV2
RDSTAT	1	0	1	1	0	0	0	0
	BUSYB3	BUSYB2	BUSYB1	BUSYB0	NCR3	NCR2	NCR1	NCR0
RDVER	1	0	1	1	0	1	0	0
	VER7	VER6	VER5	VER4	VER3	VER2	VER1	VER0
RDERR	1	0	1	1	1	0	0	0
	OSCERR	RSTERR	WDTERR	ROMERR	SPDERR	TSDERR	DCDERR	WCMERR
OUTSTAT	1	1	0	0	0	0	0	0
	0	PORT	STA1	STA0	CH3	CH2	CH1	CH0
FADR2	1	1	0	0	0	1	0	0
	0	0	C1	C0	F11	F10	F9	F8
	F7	F6	F5	F4	F3	F2	F1	F0
PLAY2	1	1	0	0	1	0	0	0
	0	0	C1	C0	F11	F10	F9	F8
	F7	F6	F5	F4	F3	F2	F1	F0
SAFE	1	1	0	1	0	0	0	0
	OSCEN	RSTEN	WDTEN	ROMEN	SPDEN	TSDEN	DCDEN	WCMEN
ERRCL	1	1	1	1	1	1	1	1

- Description of Command Functions

◆ PUP command

・ Command

0	0	0	0	0	0	0	WCM

The PUP command shifts from the power-down state to the command standby state.
Since only the PUP command is accepted when the LSI is in the power-down state, the command is ignored if another command is input.
To return to the power-down mode, enter the PDWN command.

The WCM bit is used to set the mode for inputting command and data two-times. When this bit is set to "1", the subsequent command and data inputs are set to the two-times input mode, and the command is accepted only when they match.
If they do not match, the accepted command is discarded. Refer to the "RDSTAT command", "OUTSTAT command", and "SAFE command" for handling when a mismatch occurs.

WCM	Description
0	Do not use input mode two-times. (Initial value)
1	Use the two-times input mode

For the power-up timing by the PUP command, refer to the "Power-up timing" in the timing chart.

◆ AMODE command

・ Command

0	0	0	0	0	1	DAMP	HPF	1st byte
FAD	DAG1	DAG0	AIG1	AIG0	AEN1	AEN0	POP	2nd byte

The AMODE command sets the analog part.
The AMODE command is ignored during power-down, power-up transition, power-down transition and playback sound.
When the PDWN command is input while powering up the analog parts, the LSI power downs without pop noise suppression. When power down with POP noise suppression, to set the PDWN command after powering down with AMODE command.
To perform power-down under a setting condition that differs from the power-up condition of the analog unit, set the AMODE command to set the power-down condition again.
To power up the analog part, set the CVOL command to 00h (initial value) and then enter the AMODE command.
The settings are initialized when the reset is released or when the PDWN command is inputted.

Each setting is as follows.

DAMP	Description
0	Use Class AB amplifier for speaker amplifier output.
1	Use Class D amplifier for speaker amplifier output.

When using line amplifier and using analog mixing from the AIN pin, set DAMP = "0" (Class AB amplifier is used).

HPF	Description
0	No high-pass filter is used.
1	Use a high-pass filter with a cut-off frequency of 200Hz

FAD	Description
0	Fade-out is not processed when inputting STOP command.
1	Fade out when inputting STOP command

The fade-out processing BUSYB signal becomes "L" and becomes "H" after processing is completed.

DAG1	DAG0	Description
0	0	Internal DAC signal input OFF
0	1	Internal DAC signal input ON (-6 dB)
1	0	Internal DAC signal input ON (0dB)
1	1	Internal DAC signal input ON (0dB) (setting prohibited)

The setting is enabled in the speaker amplifier output mode when using Class AB amplifier.
Refer to the "Volume Settings" in the "Function description".

AIG1	AIG0	Description
0	0	Analog input from the AIN pin OFF
0	1	Analog input from AIN pin ON (-6 dB)
1	0	Analog input from AIN pin ON (0dB)
1	1	Analog input from AIN pin ON (0dB) (setting prohibited)

Input the sound signals to the AIN pin after CBUSYB pin becomes "H" by the AMODE command.
The setting is enabled in the speaker amplifier output mode only when using Class AB amplifier.
Refer to the "Volume Settings" in the "Function description".

POP	Description
0	Without pop noise suppression
1	With pop noise suppression

This bit is valid when line amplifier output is selected.
When power up with pop noise suppression, the line amplifier output rises from the DGND level to the SG level at the specified time (tPUPA2).When power down with pop noise suppression, the line amplifier output falls from the SG level to the DGND level at the specified time (tPDA2).
When power up without pop noise suppression, the line amplifier output rises from the DGND level to the SG level at the specified time (tPUPA3).When power down without pop noise suppression, the line amplifier output falls from the SG level to the DGND level at the specified time (tPDA3).

The settings of the AEN1/AEN0/POP bits for power-down and power-up of the analog section when the speaker amplifier output and line amplifier output are as follows.

Mode	AEN1	AEN0	POP	Description
Speaker amplifier output*2 (class AB/class D)	0	0	*1	In the power-down state or changeover to the power-down state.
	0	1	*1	In the power-up state or changeover to the power-up state
Line amplifier output (When using SPP pin)	0	0	0	In the power-down state or changeover to the power-down state without Pop Noise Suppression
	1	0	0	In the power-up state or changeover to the power-up state without Pop Noise Suppression
	0	0	1	In the power-down state or changeover to the power-down state with pop noise suppression
	1	0	1	In the power-up state or changeover to the power-up state with pop noise suppression

*1 Settings can be enabled for both 0 and 1.
*2 Do not set AEN1=”1” when using class D amplifier with speaker amplifier output (DAMP=”1”).

Pin states at AMODE power-down are as follows.

Analog output pin	Condition
V_{DDL}	2.5V(typ)
SG	DGND
SPM	HiZ
SPP	SPGND

The timing of AMODE command is shown in the timing chart.
"Speaker amplifier power-up timing (DAMP bit "0", AEN1 bit "0", AEN0 bit "0"→ "1")"
"Speaker amplifier power-up timing (DAMP bit "1", AEN1 bit "0", AEN0 bit "0"→ "1")"
"Line amplifier power-up timing (DAMP bit = "0", POP bit = "1", AEN1 bit = "0" → "1", AEN0 bit = "0") "
"Line amplifier power-up timing (DAMP bit = "0", POP bit = "0", AEN1 bit = "0" → "1", AEN0 bit = "0")"
"Speaker amplifier power-down timing (DAMP bit "0", AEN1 bit "0", AEN0 bit "1"→"0")"
"Speaker amplifier power-down timing (DAMP bit "1", AEN1 bit "0", AEN0 bit "1"→"0")"
"Line amplifier power-down timing (DAMP bit = "0", POP bit = "1", AEN1 bit = "1" → "0", AEN0 bit = "0")"
"Line amplifier power-down timing (DAMP bit = "0", POP bit = "0", AEN1 bit = "1" → "0", AEN0 bit = "0")"

◆ AVOL command

・ Command

0	0	0	0	1	0	0	0	1st byte
0	0	AV5	AV4	AV3	AV2	0	0	2nd byte

The AVOL command sets the volume of the speaker amplifier. This command can be input regardless of the NCR signal status.
The initial value after reset release is set to-4.0dB. Also, the setting values of the AVOL command are retained when the STOP command is inputted, but they are initialized when the power is down.

AV5-AV2	Description	AV5-AV2	Description
F	+12.0dB	7	-8.0dB
E	+10.0dB	6	-12.0dB
D	+8.0dB	5	-18.0dB
C	+6.0dB	4	-26.0dB
B	+4.0dB	3	-34.0dB
A	+2.0dB	2	Prohibited
9	+0.0dB	1	Prohibited
8	-4.0dB (initial value)	0	OFF

For timing of the AVOL command, refer to the "Change volume timing by AVOL command" in the timing chart.

◆ FADE command

・ Command

0	0	0	0	1	1	0	0	1st byte
0	0	0	0	FCON2	FCON1	FCON0	FADE	2nd byte

The FADE command sets the Fade function. This command can be input regardless of the NCR signal status.
By using the fade function, the volume changes stepwise when the volume is changed by the CVOL command.

FADE	Description
0	Fade function disabled (initial value)
1	Fade function enabled

FCON2 to FCON0 set the volume that changes at every unit-time (sampling group period *1) when the volume is changed to the volume set by the CVOL command or the PAN command.

FCON2	FCON1	FCON0	Description
0	0	0	Volume change in 0 dB × 128/32768 steps
0	0	1	Volume change in 0 dB × 64/32768 steps
0	1	0	Volume change in 0 dB × 32/32768 steps
0	1	1	Volume change in 0 dB × 16/32768 steps
1	0	0	Volume change in 0 dB × 8/32768 steps
1	0	1	Volume change in 0 dB × 4/32768 steps
1	1	0	Volume change in 0 dB × 2/32768 steps
1	1	1	Volume change in 0 dB × 1/32768 steps

The smaller the voltage step that changes for each sampling frequency group, the less the pop noise, but the longer the transition time until the set volume is reached. The transition time is expressed by the following equation.

Volume-transition time for CVOL command.

=|[Current CVOL setting]-[New CVOL setting]|
× [Sampling-frequency group *1]
× {264 ÷ (256 ÷ 2^[FCON2-FCON0 setting])}*2

*1 Sampling frequency group
At 10.7/21.3kHz: 23.44µs
At 6.4/12.8/25.6kHz: 39.06µs
At 8.0/16.0/32.0kHz: 31.25µs
At 11.025/22.05/44.1kHz: 22.68µs
At 12.0/24.0/48.0kHz: 20.83µs
*2 Rounding up after the decimal point.

For the timing of the FADE command, refer to the "FADE command timing" in the timing chart.

◆ FDIRECT command

・ Command

0	0	0	1	0	0	0	0	1st byte
PRT7	PRT6	PRT5	PRT4	PRT3	PRT2	PRT1	PRT0	2nd byte

The FDIRECT command controls accesses to the serial flash memory using the clock-synchronous serial interface. Input the command after inputting the PUP command.

If the protection code of the flash memory area is not 0x69 and the protection codes (PRT7 to PRT0) entered in the second byte match the protection code set when creating sound ROM data, the serial flash memory access mode is entered. After that, the flash memory can be accessed using the clock synchronous serial interface.
If the protection code set when creating sound ROM data is 0x69, the flash memory does not change to serial flash memory access mode even if the code matches.

To cancel the serial flash memory access mode, insert a reset (RESETB = "L") and conduct initialization or turn off the power supply.

For the protection codes of the flash memory area, refer to the "Speech LSI Utility Setting Items".
For the timing of the FDIRECT command, refer to the "FDIRECT command timing" in the timing chart.

◆ WDTCL command

・ Command

0	0	0	1	0	1	0	0

The WDTCL command clears the watchdog timer counter (WDT counter). This command can be input regardless of the NCR signal status.

For information about the operation of the watchdog timer, refer to the "Misoperation detection and failure detection functions (Watchdog timer overflow detection)" in the "Function description".
For the timing of WDTCL command, refer to the "WDTCL command timing" in the timing chart.

◆ PDWN command

・ Command

0	0	1	0	0	0	0	0

The PDWN command is used to shift from the command standby state to the power-down state. The various settings are initialized, so the initial settings are required after power-up. It is invalid when the BUSYB signals of any channels are "L".

After inputting the PDWN command, oscillation stops following the elapse of the command processing time (tPD) .

The states of the analog output pins during power-down are shown below.

Analog output pin	Condition
V_{DDL}	DGND
SG	DGND
SPM	HiZ
SPP	SPGND

For the power-down timing by PDWN command, refer to the "Power-Down timing" in the timing chart.

◆ FADR command

・ Command

0	0	1	1	F9	F8	C1	C0	1st byte
F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

The FADR command sets the channels and phrases to be played. This command can be input when the NCR signal of the corresponding channel is "H" level.
Playback is started by the START command after the playback phrases of each channel are specified.
The phrases (F9-F0) to be played back are specified when creating sound ROM data. Set the phrase specified when creating.
This command can only set up to 0 to 1023 phrases. To specify 1024 phrases or more, use FADR2 command.

The channel settings are as follows:

C1	C0	Description
0	0	Channel 0
0	1	Channel 1
1	0	Channel 2
1	1	Channel 3

For the timing of the FADR command, refer to the "Setting playback phrases using FADR command" in the timing chart.

◆ PLAY command

・ Command

0	1	0	0	F9	F8	C1	C0	1st byte
F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

The PLAY command is played by specifying channels and phrases. This command can be input when the NCR signal of the corresponding channel is "H" level.
The phrases (F9-F0) to be played back are specified when creating sound ROM data. Set the phrase specified when creating. This command can only set up to 0 to 1023 phrases. To specify 1024 phrases or more, use PLAY2 command.

The channel settings are as follows:

C1	C0	Description
0	0	Channel 0
0	1	Channel 1
1	0	Channel 2
1	1	Channel 3

For the playback start timing by the PLAY command, refer to the "Playback start timing by PLAY command" in the timing chart.
For the timing of continuous playback, refer to the "Continuous playback timing by PLAY command" in the timing chart.

◆ START command

・ Command

0	1	0	1	CH3	CH2	CH1	CH0	1st byte

The START command starts playing back the specified channels. Specify the phrase to be played by the FADR command prior to entering the START command. Setting the CH0 to CH3 bit to 1 plays back the corresponding channel. This command can be input when the NCR signal of the corresponding channel is "H" level.

The channel settings are as follows:

Channeled	Description
CH0	When this bit is set to 1, channel 0 is played back.
CH1	When this bit is set to 1, channel 1 is played back.
CH2	When this bit is set to 1, channel 2 is played back.
CH3	When this bit is set to 1, channel 3 is played back.

Be sure to specify one of the channels for the channel setting (CH0-CH3).
Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

For the playback start timing by the START command, refer to the "Playback start timing by START command" in the timing chart.
For the timing of continuous playback, refer to the "Continuous playback timing by START command" in the timing chart.

◆ STOP command

・ Command

0	1	1	0	CH3	CH2	CH1	CH0

1st byte

The STOP command stops playing back the specified channel. Setting the CH0 to CH3 bit to "1" stops playback of the corresponding channel. When the corresponding channel stops playing back, the NCR and BUSYB signals become "H".

The STOP command can be input regardless of the status of the NCR during playback operation. However, following the elapse of CBUSYB "L" level output time 3 (tCB3), input the next command after confirming that the BUSYB signal becomes "H".
If the BUSYB signal does not become "H", enter the STOP command again.
Refer to the "Playback stop flow" in the command flowchart for more information.

The channel settings are as follows:

Channeled	Description
CH0	Setting this bit to 1 stops channel 0.
CH1	Setting this bit to 1 stops channel 1.
CH2	Setting this bit to 1 stops channel 2.
CH3	Setting this bit to 1 stops channel 3.

Be sure to specify one of the channels for the channel setting (CH0-CH3).
Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

For the timing of the STOP command, refer to the "STOP command (when the FAD bit is "L")" and "STOP command (when the FAD bit is "H")" in the timing chart.

◆ MUON command

・ Command

0	1	1	1	CH3	CH2	CH1	CH0	1st byte
M7	M6	M5	M4	M3	M2	M1	M0	2nd byte

The MUON command inserts silence between two phrases to be played. This command can be inputted when the NCR signal of the corresponding channel is "H" level.
Repeated playing back (the SLOOP command) of the MUON command is not possible.

The silence duration (t_{mu}) is specified by the M7-M0 bits and can be set from 20ms to 1,024ms in 252 steps at 4ms intervals.
The equation for setting the mute time (t_{mu}) is as follows.
However, set the silence setting (M7-M0) to 04h or more ($t_{mu} \geq 20ms$).

$$t_{mu}=(2^7\times(M7)+2^6\times(M6)+2^5\times(M5)+2^4\times(M4)+2^3\times(M3)+2^2\times(M2)+2^1\times(M1)+2^0\times(M0)+1)\times 4ms$$

The channel settings are as follows:

Channeled	Description
CH0	Setting this bit to 1 inserts silence into channel 0.
CH1	Setting this bit to 1 inserts silence into channel 1.
CH2	Setting this bit to 1 inserts silence into channel 2.
CH3	Setting this bit to 1 inserts silence into channel 3.

Be sure to specify one of the channels for the channel setting (CH0-CH3).
Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

For the timing of the MUON command, refer to the "Playback start timing by MUON command" in the timing chart.
For the timing of continuous playback, refer to the "Continuous playback timing by MUON command" in the timing chart.

◆ SLOOP command

・ Command

1	0	0	0	CH3	CH2	CH1	CH0	1st byte

The SLOOP command sets the repeat playback of the specified channel. Setting the CH0 to CH3 bit to 1 repeatedly plays back the corresponding channel. This command can be input when the NCR signal of the corresponding channel is "H" level.

When repeat playback is set, playback is repeatedly performed until the repeat playback setting is canceled by the CLOOP command or playback is stopped by the STOP command. Also, if the phrase has been edited, the edited phrase is played repeatedly.

The channel settings are as follows:

Channeled	Description
CH0	Setting this bit to 1 repeats playback on channel 0.
CH1	Setting this bit to 1 repeats playback on channel 1.
CH2	Setting this bit to 1 repeats playback on channel 2.
CH3	Setting this bit to 1 repeats playback on channel 3.

Be sure to specify one of the channels for the channel setting (CH0-CH3).
Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

For the timing of the SLOOP command, refer to the "Repeat playback setting/release timing by SLOOP/CLOOP command" in the timing chart.

◆ CLOOP command

・ Command

1	0	0	1	CH3	CH2	CH1	CH0	1st byte

The CLOOP command releases repeat playback of the specified channel. This command can be input regardless of the NCR signal status.
Setting the CH0 to CH3 bit to "1" cancels repeat playback of the corresponding channel. When repeat playback is released, the NCR signal becomes "H" level.

The channel settings are as follows:

Channeled	Description
CH0	Setting this bit to 1 cancels repeat playback on channel 0.
CH1	Setting this bit to 1 cancels repeat playback on channel 1.
CH2	Setting this bit to 1 cancels repeat playback on channel 2.
CH3	Setting this bit to 1 cancels repeat playback on channel 3.

Be sure to specify one of the channels for the channel setting (CH0-CH3).
Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

For the timing of the CLOOP command, refer to the "Repeat playback setting/release timing by SLOOP/CLOOP command" in the timing chart.

◆ CVOL command

・ Command

1	0	1	0	CH3	CH2	CH1	CH0	1st byte
0	CV1	CV0	CV6	CV5	CV4	CV3	CV2	2nd byte

The CVOL command sets the playback volume of the specified channel. This command can be input regardless of the NCR signal status.
Setting the CH0 to CH3 bit to 1 sets the volume of the corresponding channel.

The volume can be set at 128 levels.
The setting values are initialized when a reset is inserted (RESETB = "L") and PDWN command is input.
The CV1 and CV0 of the second bytes of the CVOL command are located at the top of the CV6 to CV2.

CV1,CV0, CV6-CV2	Description	CV1,CV0, CV6-CV2	Description	CV1,CV0, CV6-CV2	Description	CV1,CV0, CV6-CV2	Description
00	0.00dB (initial value)	08	-2.59dB	10	-6.31dB	18	-12.93dB
20	-0.07dB	28	-2.69dB	30	-6.45dB	38	-13.24dB
40	-0.14dB	48	-2.78dB	50	-6.60dB	58	-13.57dB
60	-0.21dB	68	-2.88dB	70	-6.75dB	78	-13.91dB
01	-0.28dB	09	-2.98dB	11	-6.90dB	19	-14.26dB
21	-0.36dB	29	-3.08dB	31	-7.06dB	39	-14.63dB
41	-0.43dB	49	-3.18dB	51	-7.22dB	59	-15.02dB
61	-0.50dB	69	-3.28dB	71	-7.38dB	79	-15.42dB
02	-0.58dB	0A	-3.38dB	12	-7.55dB	1A	-15.85dB
22	-0.65dB	2A	-3.49dB	32	-7.72dB	3A	-16.29dB
42	-0.73dB	4A	-3.59dB	52	-7.89dB	5A	-16.76dB
62	-0.81dB	6A	-3.70dB	72	-8.06dB	7A	-17.26dB
03	-0.88dB	0B	-3.81dB	13	-8.24dB	1B	-17.79dB
23	-0.96dB	2B	-3.92dB	33	-8.43dB	3B	-18.35dB
43	-1.04dB	4B	-4.03dB	53	-8.61dB	5B	-18.95dB
63	-1.12dB	6B	-4.14dB	73	-8.80dB	7B	-19.59dB
04	-1.20dB	0C	-4.25dB	14	-9.00dB	1C	-20.28dB
24	-1.28dB	2C	-4.37dB	34	-9.20dB	3C	-21.04dB
44	-1.36dB	4C	-4.48dB	54	-9.40dB	5C	-21.87dB
64	-1.44dB	6C	-4.60dB	74	-9.61dB	7C	-22.78dB
05	-1.53dB	0D	-4.72dB	15	-9.83dB	1D	-23.81dB
25	-1.61dB	2D	-4.84dB	35	-10.05dB	3D	-24.97dB
45	-1.70dB	4D	-4.97dB	55	-10.27dB	5D	-26.31dB
65	-1.78dB	6D	-5.09dB	75	-10.50dB	7D	-27.89dB
06	-1.87dB	0E	-5.22dB	16	-10.74dB	1E	-29.83dB
26	-1.96dB	2E	-5.35dB	36	-10.99dB	3E	-32.33dB
46	-2.04dB	4E	-5.48dB	56	-11.24dB	5E	-35.85dB
66	-2.13dB	6E	-5.61dB	76	-11.50dB	7E	-41.87dB
07	-2.22dB	0F	-5.74dB	17	-11.77dB	1F	-44.37dB
27	-2.31dB	2F	-5.88dB	37	-12.04dB	3F	-47.89dB
47	-2.41dB	4F	-6.02dB	57	-12.33dB	5F	-53.91dB
67	-2.50dB	6F	-6.16dB	77	-12.62dB	7F	OFF

The volume can also be set at 32 levels by fixing the CV1 and CV0 bits to "0".

CV6-CV2	Description	CV6-CV2	Description
00	0.00dB (initial value)	10	-6.31dB
01	-0.28dB	11	-6.90dB
02	-0.58dB	12	-7.55dB
03	-0.88dB	13	-8.24dB
04	-1.20dB	14	-9.00dB
05	-1.53dB	15	-9.83dB
06	-1.87dB	16	-10.74dB
07	-2.22dB	17	-11.77dB
08	-2.59dB	18	-12.93dB
09	-2.98dB	19	-14.26dB
0A	-3.38dB	1A	-15.85dB
0B	-3.81dB	1B	-17.79dB
0C	-4.25dB	1C	-20.28dB
0D	-4.72dB	1D	-23.81dB
0E	-5.22dB	1E	-29.83dB
0F	-5.74dB	1F	-44.37dB

The channel settings are as follows:

Channeled	Description
CH0	Setting this bit to 1 set the volume of channel 0.
CH1	Setting this bit to 1 set the volume of channel 1.
CH2	Setting this bit to 1 set the volume of channel 2.
CH3	Setting this bit to 1 set the volume of channel 3.

Be sure to specify one of the channels for the channel setting (CH0-CH3). When multiple channels are specified, the volume of the specified channels is set.
Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

For timing of the CVOL command, refer to the "Change volume timing by CVOL command" in the timing chart.

◆ RDSTAT command

・ Command

1	0	1	1	0	0	0	0	1st byte

The RDSTAT command reads the internal operating states. This command can be input regardless of the NCR signal status. When reading the status of the second byte after command input, set the SI pin to "L".

The internal operating states read in the second byte are as follows:

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
Output data	BUSYB3	BUSYB2	BUSYB1	BUSYB0	NCR3	NCR2	NCR1	NCR0

The NCR signal outputs "L" during command processing and playback standby, and outputs "H" in other states.
The BUSYB signal outputs "L" during command processing and playback sound, and outputs "H" in other states.

D7 to D0	Description
BUSYB3	BUSYB outputs of channel 3
BUSYB2	BUSYB outputs of channel 2
BUSYB1	BUSYB outputs of channel 1
BUSYB0	BUSYB outputs of channel 0
NCR3	NCR output of channel 3
NCR2	NCR output of channel 2
NCR1	NCR output of channel 1
NCR0	NCR output of channel 0

For the timing of the RDSTAT command, refer to the "RDSTAT command timing" in the timing chart.

◆ RDVER command

・ Command

1	0	1	1	0	1	0	0

1st byte

The RDVER command read sound ROM information. This command can be input regardless of the NCR signal status. When reading the sound ROM information in the second byte after command input, set the SI pin to "L".

The sound ROM information read in the second byte is as follows:

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
Output data	VER7	VER6	VER5	VER4	VER3	VER2	VER1	VER0

Sound ROM information can be set by using dedicated tool (Speech LSI Utility) when creating sound ROM data.

For the timing of the RDVER command, refer to the "RDVER command timing" in the timing chart.

◆ RDERR command

・ Command

1	0	1	1	1	0	0	ERSEL	1st byte

The RDERR command read misoperation detection and failure detection status. This command can be input regardless of the NCR signal status. When reading error information in the second byte after command input, set the SI pin to "L".

If the outputs of misoperation detection and failure detection are selected by OUTSTAT command, and the read data is all "L" even though STATUS1 or STATUS2 pin is "H", the read data cannot be read normally. Be sure to read it again.

The internal operating states read in the second byte are as follows:

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
Output data	OSCERR	RSTERR	WDTERR	ROMERR	SPDERR	TSDERR	DCDERR	WCMERR

Misoperation detection and failure detection status are as follows.

Error signal	Description
WCMERR	This bit is set to "1" when an error of the command is detected.
DCDERR	This bit is set to "1" when the disconnection of the speaker connected to the SPP and SPM pins is detected.
TSDERR	This bit is set to "1" when the LSI temperature becomes 130°C or higher.
SPDERR	This bit is set to "1" when the SPP pin and the SPM pin are short-circuited, or when the SPP pin or the SPM pin is short-circuited to GND.
ROMERR	This bit is set to 1 when an error is detected in the flash memory.
WDTERR	This bit is set to "1" when the first overflow of the watchdog timer counter occurs.
RSTERR	This bit is set to "1" when the second overflow of the watchdog timer counter occurs. Alternatively, this bit is set to "1" when the RST counter, which starts operation by any of the error detections, overflows.
OSCERR	This bit is set to "1" when the clock input from the crystal resonator or ceramic resonator is stopped.

For details on misoperation detection and failure detection, refer to the "Misoperation detection and failure detection functions" in the "Function description".
For the timing of the RDERR command, refer to the "RDERR command timing" in the timing chart.

◆ OUTSTAT command

・ Command

1	1	0	0	0	0	0	0	1st byte
0	PORT	STA1	STA0	CH3	CH2	CH1	CH0	2nd byte

The OUTSTAT command selects the internal operating states output to the STATUS1 pin and STATUS2 pin.
This command can be input regardless of the NCR signal status.

PORT	Description
0	STATUS1 Pin setting
1	STATUS2 Pin setting

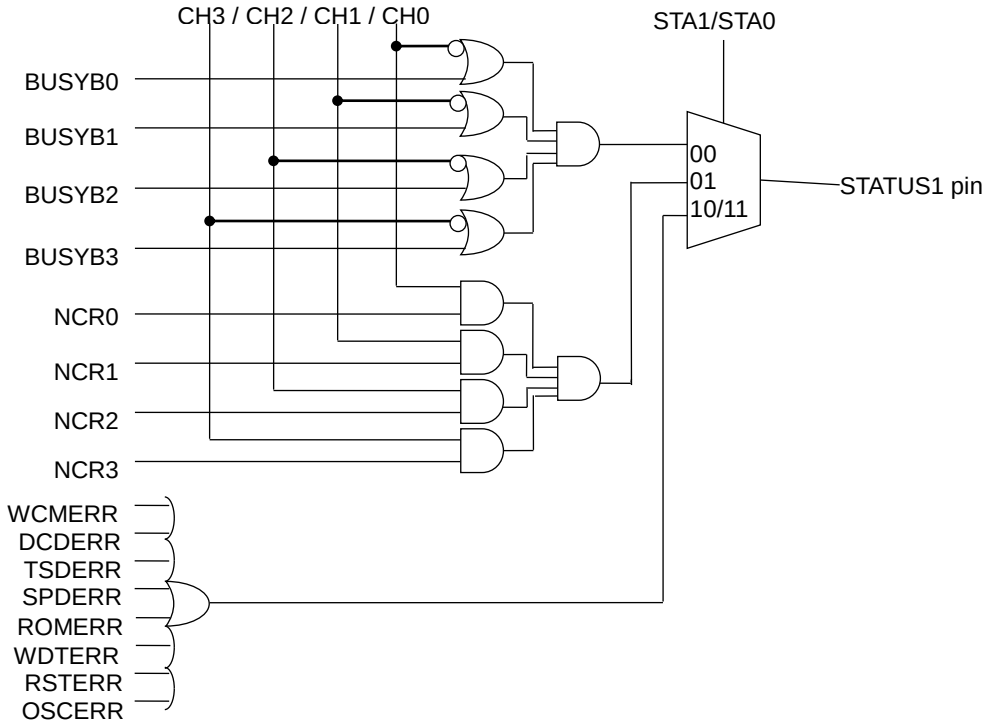
If the STATUS2 pin is set after the STATUS1 pin is set, the STATUS1 pin setting is retained.
In the initial setting, the NCR of channel 0 is selected for the STATUS1 pin, and the BUSYB of channel 0 is selected for the STATUS2 pin.

STA1	STA0	Description
0	0	BUSYB
0	1	NCR
1	0	Misoperation detection and Failure Detection
1	1	

Channeled	Description
CH0	Setting this bit to 1 selects channel 0.
CH1	Setting this bit to 1 selects channel 1.
CH2	Setting this bit to 1 selects channel 2.
CH3	Setting this bit to 1 selects channel 3.

Channel settings are enabled when BUSYB or NCR is specified in the STA1/STA0. Multiple channels can also be set.

The relation between the STATUS1 pin and the STA1/STA0/CH3/CH2/CH1/CH0 are shown below.



For the timing of the OUTSTAT command, refer to the "OUTSTAT command timing" in the timing chart.

◆ FADR2 command

・ Command

1	1	0	0	0	1	0	0	1st byte
0	0	C1	C0	F11	F10	F9	F8	2nd byte
F7	F6	F5	F4	F3	F2	F1	F0	3rd byte

The FADR2 command sets the channels and phrases to be played. This command can be input when the NCR signal of the corresponding channel is "H" level.
Playback is started by the START command after the playback phrases of the channels are specified.
The phrases (F11-F0) to be played back are specified when creating sound ROM data. Set the phrase specified when creating.

The channel settings are as follows:

C1	C0	Description
0	0	Channel 0
0	1	Channel 1
1	0	Channel 2
1	1	Channel 3

When the number of phrases to be played is 1024 or less, the channels and phrases can be specified by FADR command.

For the timing of the FADR2 command, refer to the "Setting timing of playback phrases by FADR2 command" in the timing chart.

◆ PLAY2 command

・ Command

1	1	0	0	1	0	0	0	1st byte
0	0	C1	C0	F11	F10	F9	F8	2nd byte
F7	F6	F5	F4	F3	F2	F1	F0	3rd byte

The PLAY2 command is played by specifying channels and phrases. This command can be input when the NCR signal of the corresponding channel is "H" level.
The phrases (F11-F0) to be played back are specified when creating sound ROM data. Set the phrase specified when creating.

The channel settings are as follows:

C1	C0	Description
0	0	Channel 0
0	1	Channel 1
1	0	Channel 2
1	1	Channel 3

When the number of phrases to be played is 1024 or less, the channels and phrases can be specified by PLAY command.

For the playback start timing by the PLAY2 command, refer to the "Playback start timing by PLAY2 command" in the timing chart.

◆ SAFE command

・ Command

1	1	0	1	0	0	0	0	1st byte
OSCEN	RSTEN	WDTEN	ROMEN	SPDEN	TSDEN	DCDEN	WCMEN	2nd byte

The SAFE command is used to set the operation of the misoperation detection function and the failure detection function. The initial value is the operation stop state ("0"). When this bit is set to "1", operation starts.

Error setting	Description
WCMEN	Set the command error detection.
DCDEN	Set the disconnection detection of the speakers connected to the SPP and SPM pins.
TSDEN	Set the LSI temperature error detection.
SPDEN*2	Set the detection of short circuit between the SPP pin and the SPM pin.
ROMEN	Set error detection of flash memory.
WDTEN*1	Operate the watchdog timer and set overflow detection.
RSTEN*1	Operate the RST counter and set overflow detection, when any error is detected.
OSCEN	Enable the error output for the stop detection of clock input from a crystal resonator or ceramic resonator.

*1 Do not set WDTEN and RSTEN to "1" at the same time. If these bits are set to "1" at the same time, only the RSTEN bit is set to "1".

*2 Set SPDEN to “1” when mixing and playing using class D speaker amplifier. Refer to “Class D amplifier precaution on mixing” in the “Function description”.

For details on misoperation detection and failure detection, refer to the "Misoperation detection and failure detection functions" in the function description.
For the timing of the SAFE command, refer to the "SAFE command timing" in the timing chart.

◆ ERRCL command

・ Command

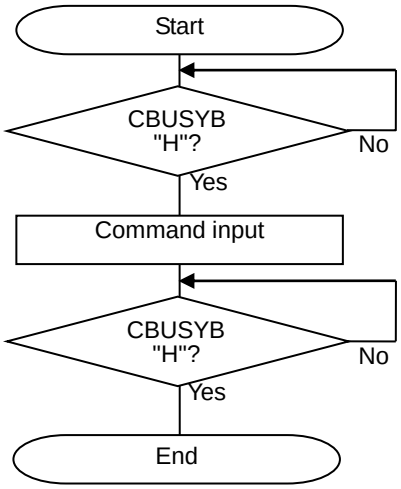
1	1	1	1	1	1	1	1

The ERRCL command is a command that clears error bits that can be read by the RDERR command. This command can be input regardless of the NCR signal status.
However, if the error continues, the error bit remains in the error status even if the ERRCL command is entered.

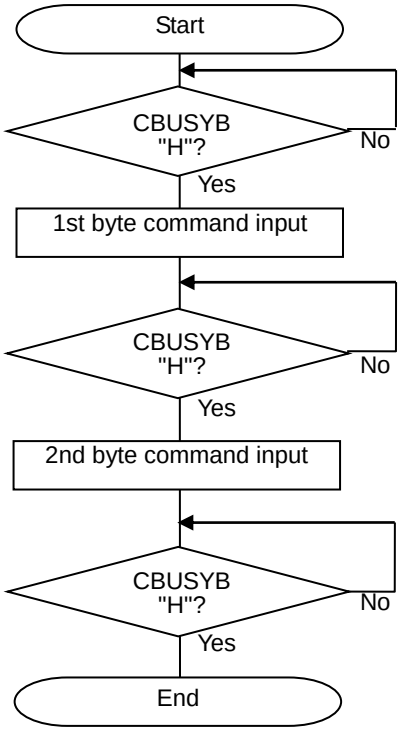
For the timing of the ERRCL command, refer to the "ERRCL command timing" in the timing chart.

■ Command Flowchart

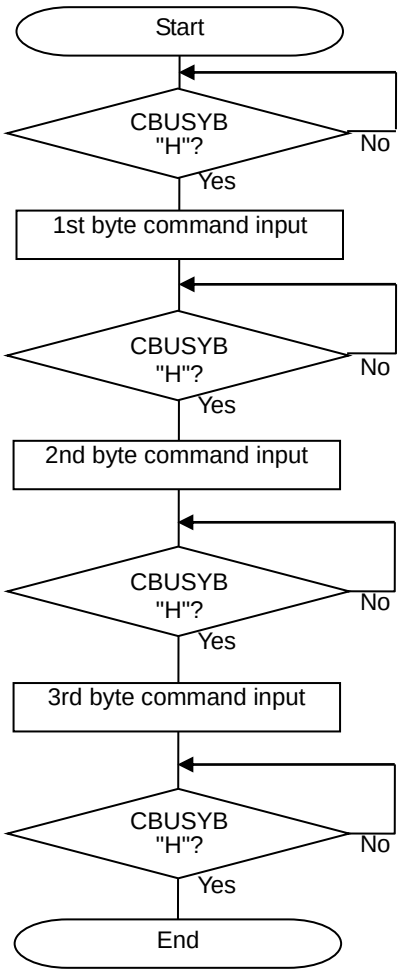
- 1-byte command input flow (Applies to PUP, WDTCL, PDWN, START, STOP, SLOOP, CLOOP, and ERRCL commands.)



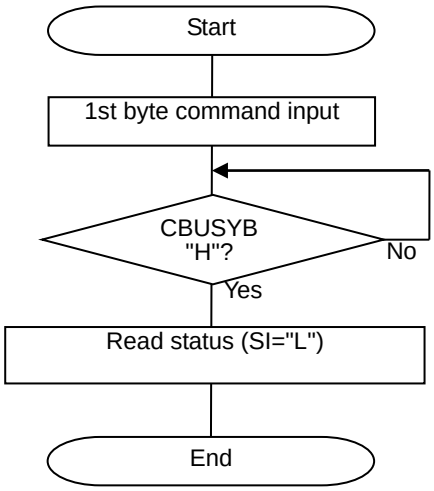
- 2-byte command input flow (Applies to AMODE, AVOL, FADE, FDIRECT, FADR, PLAY, MUON, CVOL, OUTSTAT, SAFE commands.)



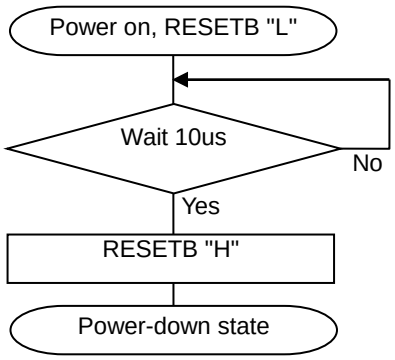
- 3-byte command input flow (Applies to FADR2, PLAY2 command)



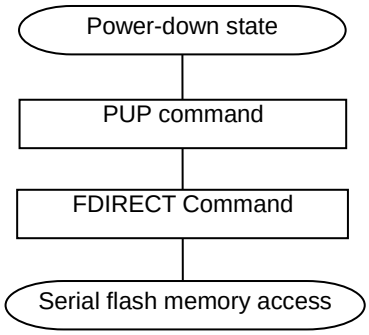
- Read flow (Applies to RDSTAT, RDVER, RDERR commands)



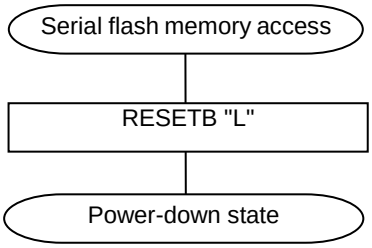
- Power-on flow



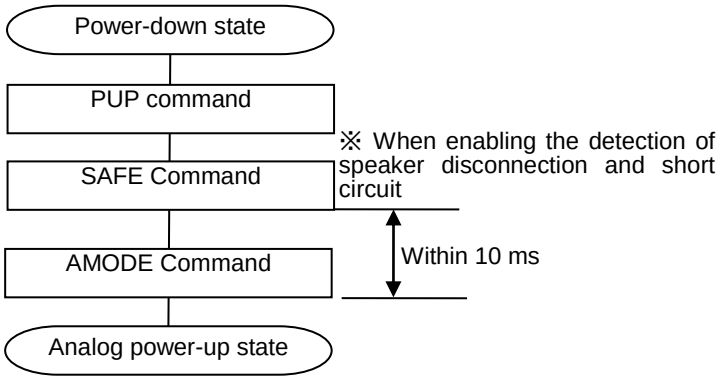
- MCU command interface Sserial flash memory access migration



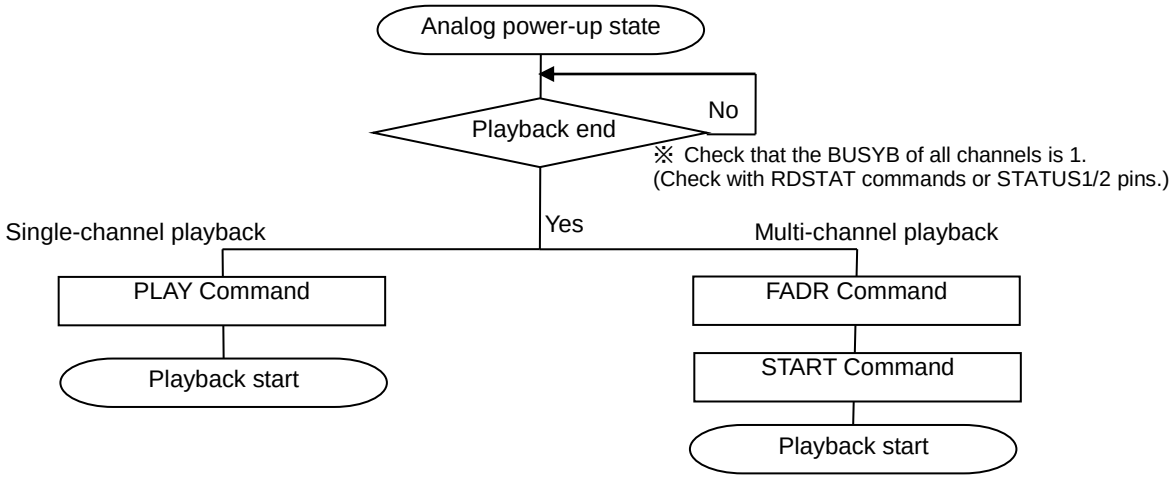
- MCU command interface serial flash memory access cancel



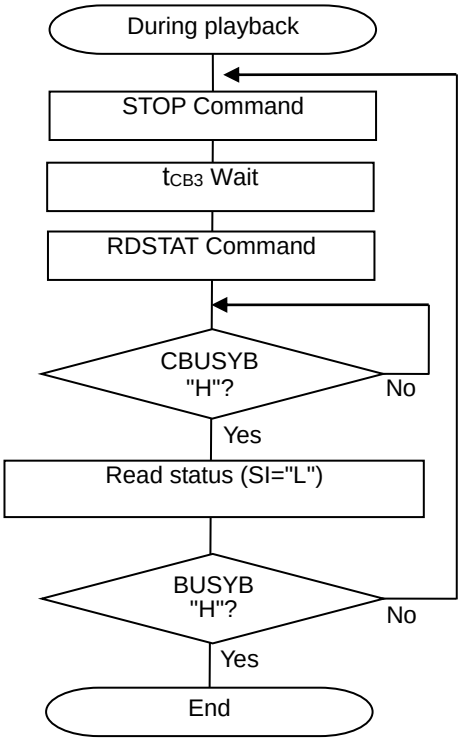
- Analog power-up flow



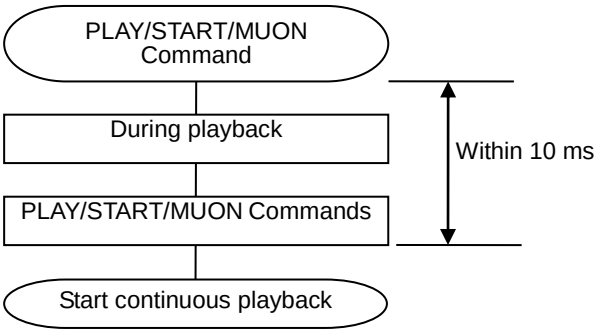
- Playback start flow



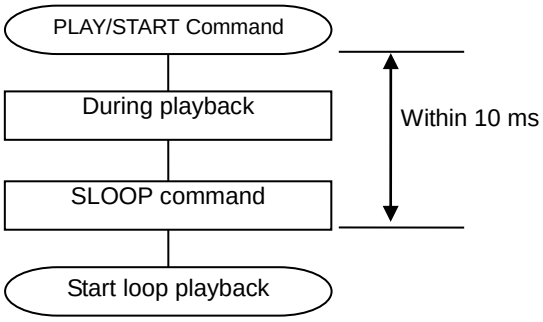
- Playback stop flow



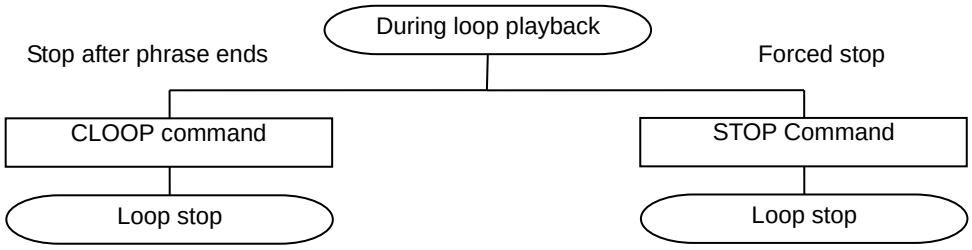
- Continuous playback flow



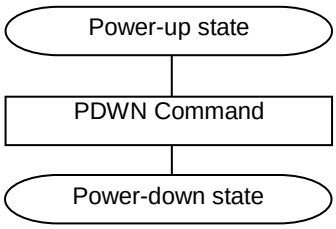
- Loop playback start flow



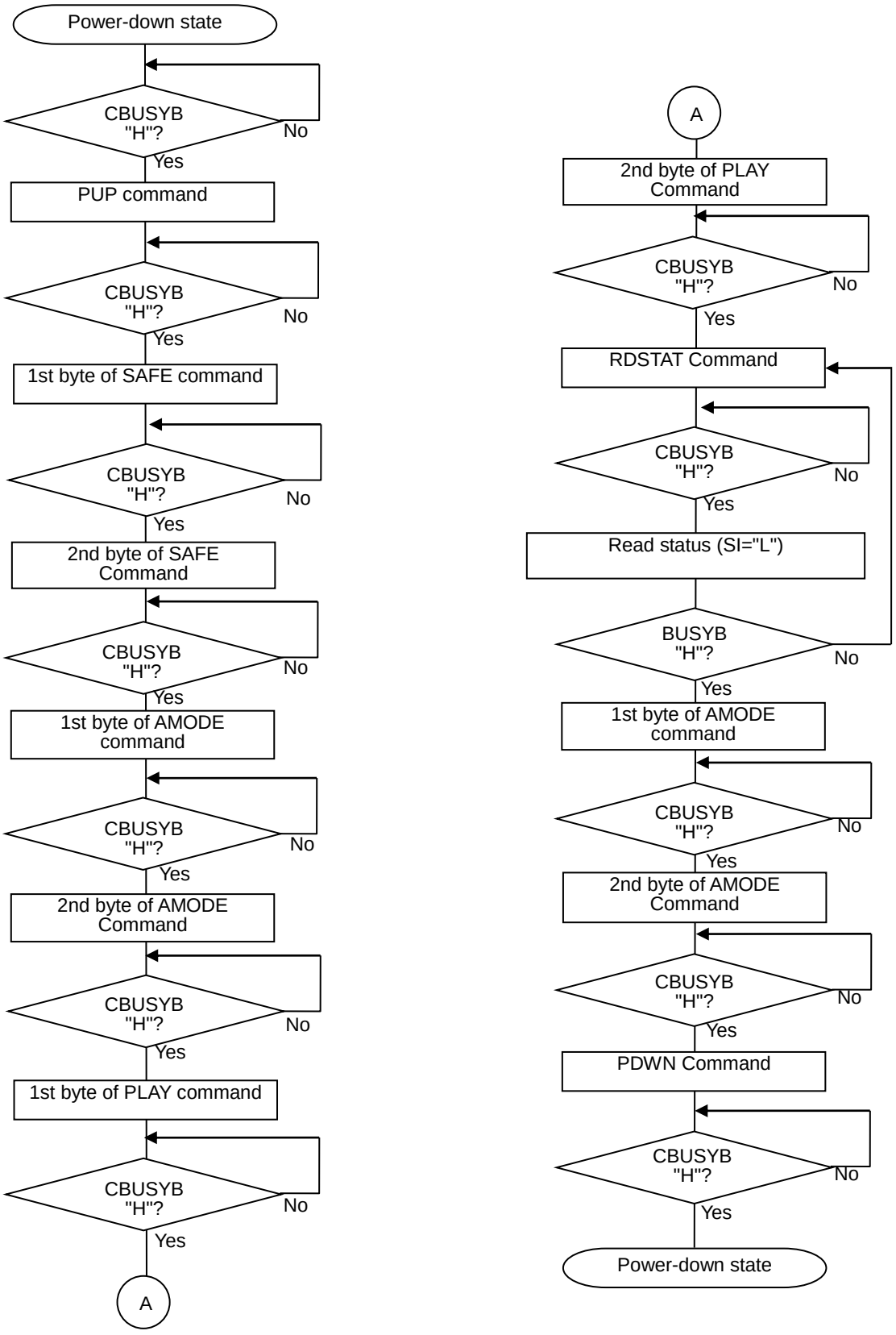
- Loop playback stop flow



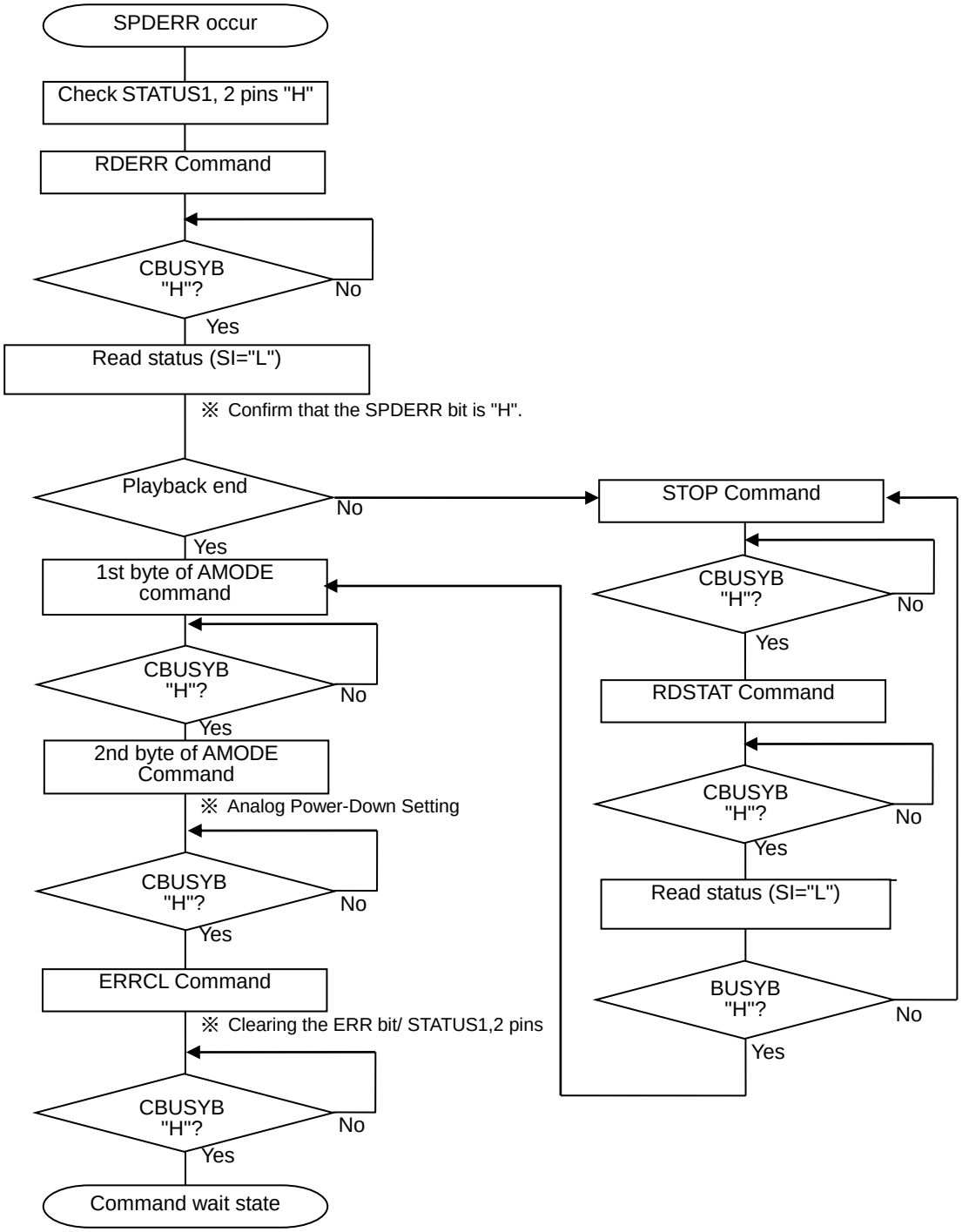
- Power-down flow



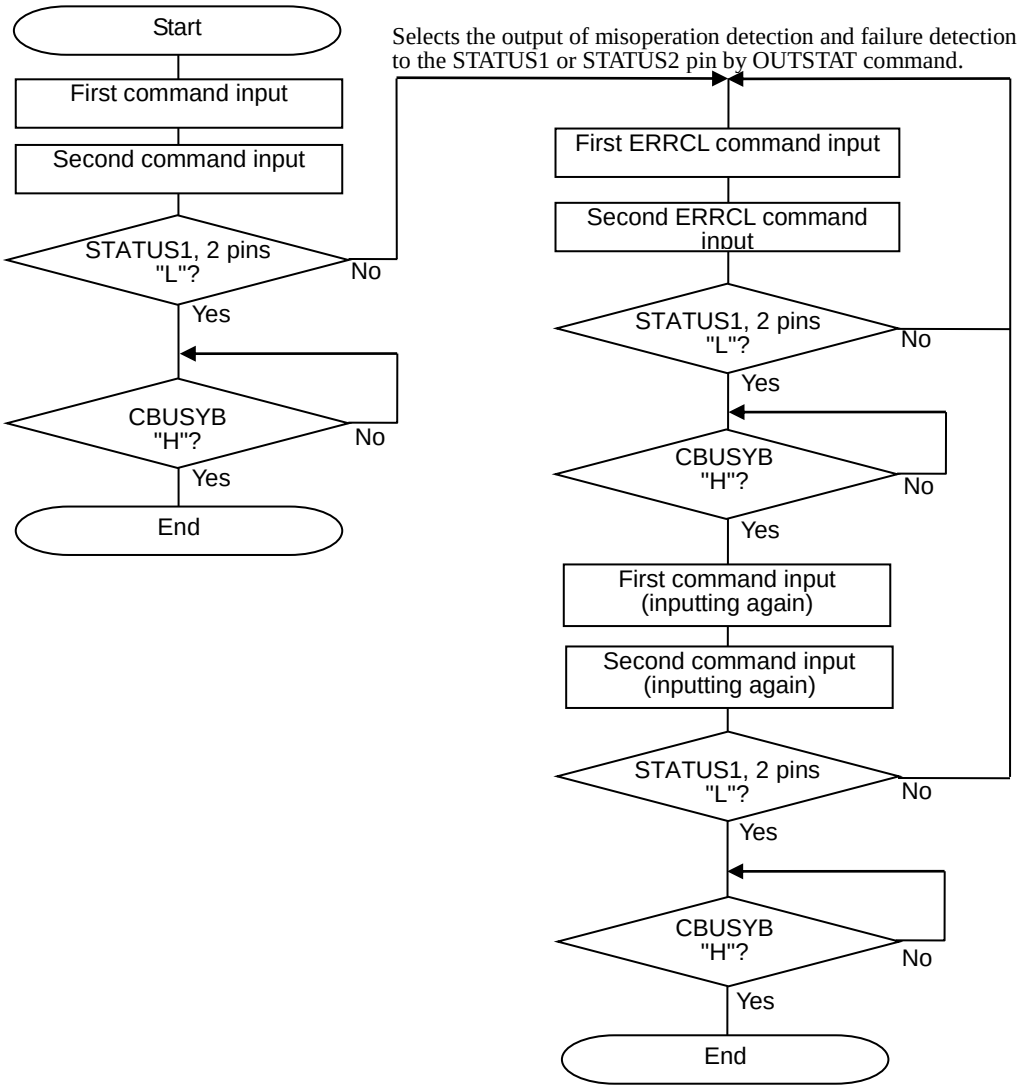
- Detailed flow of "Power-up → Playback → Power-down"



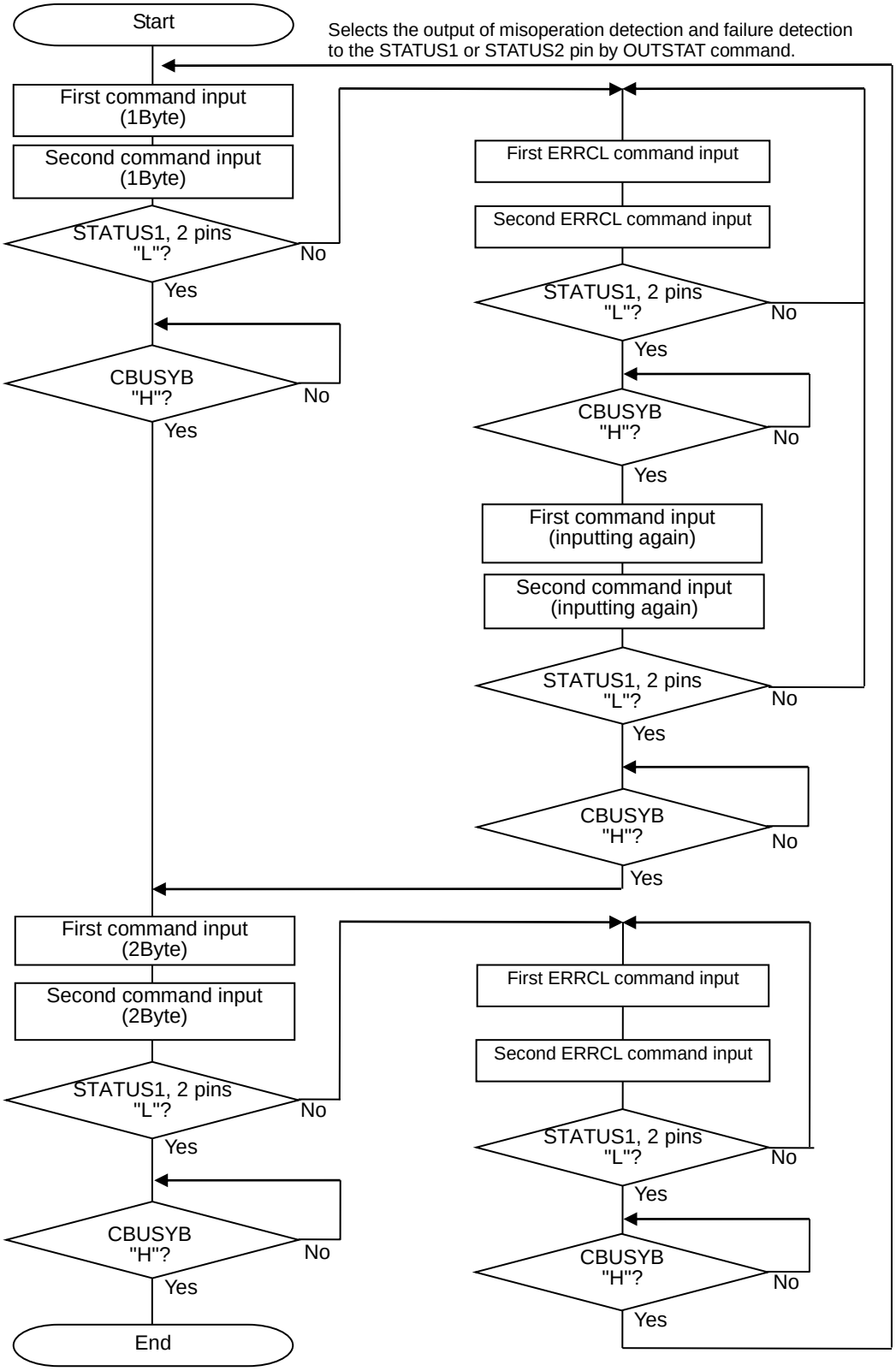
- Processing flow for speaker short detection



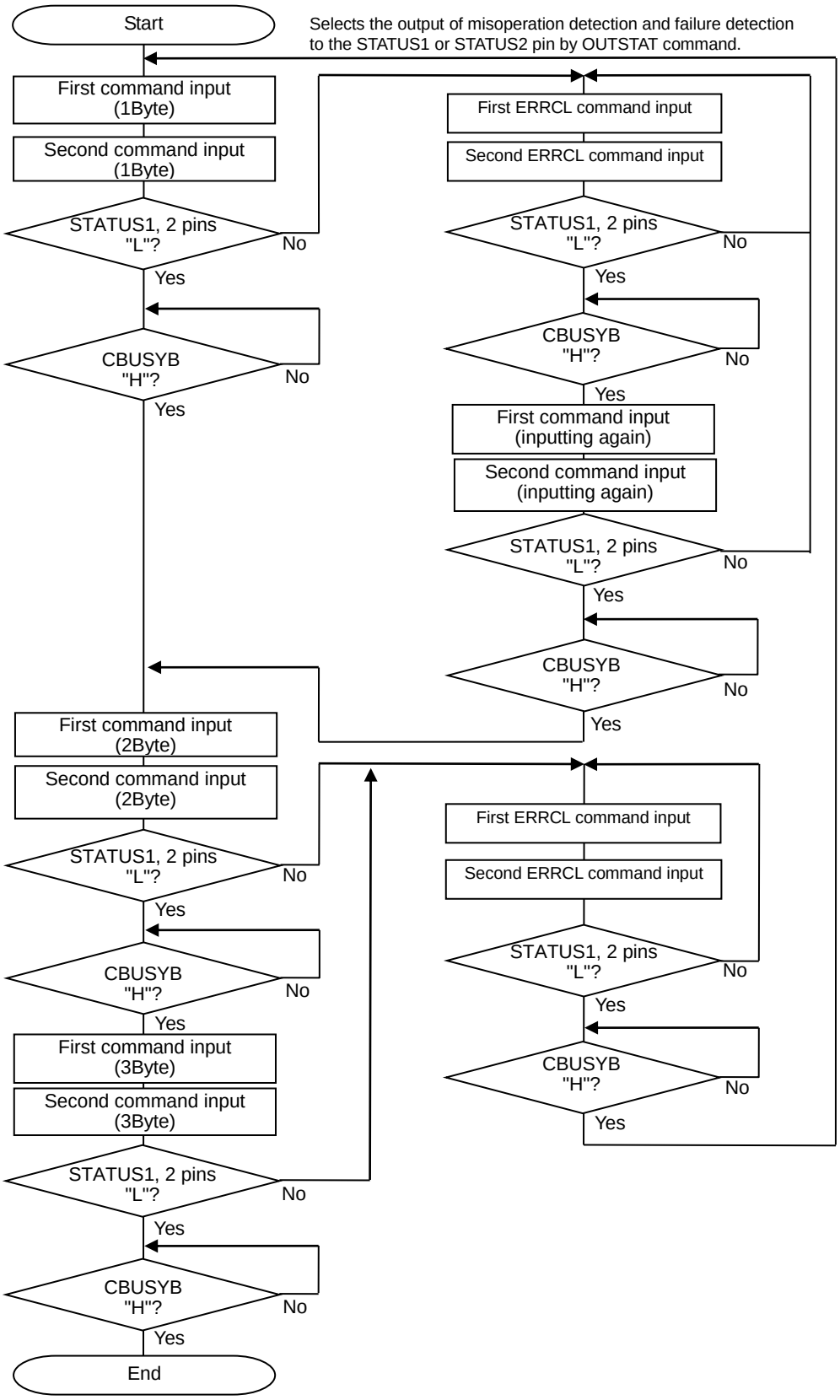
- 1-byte command input flow in two-times input mode



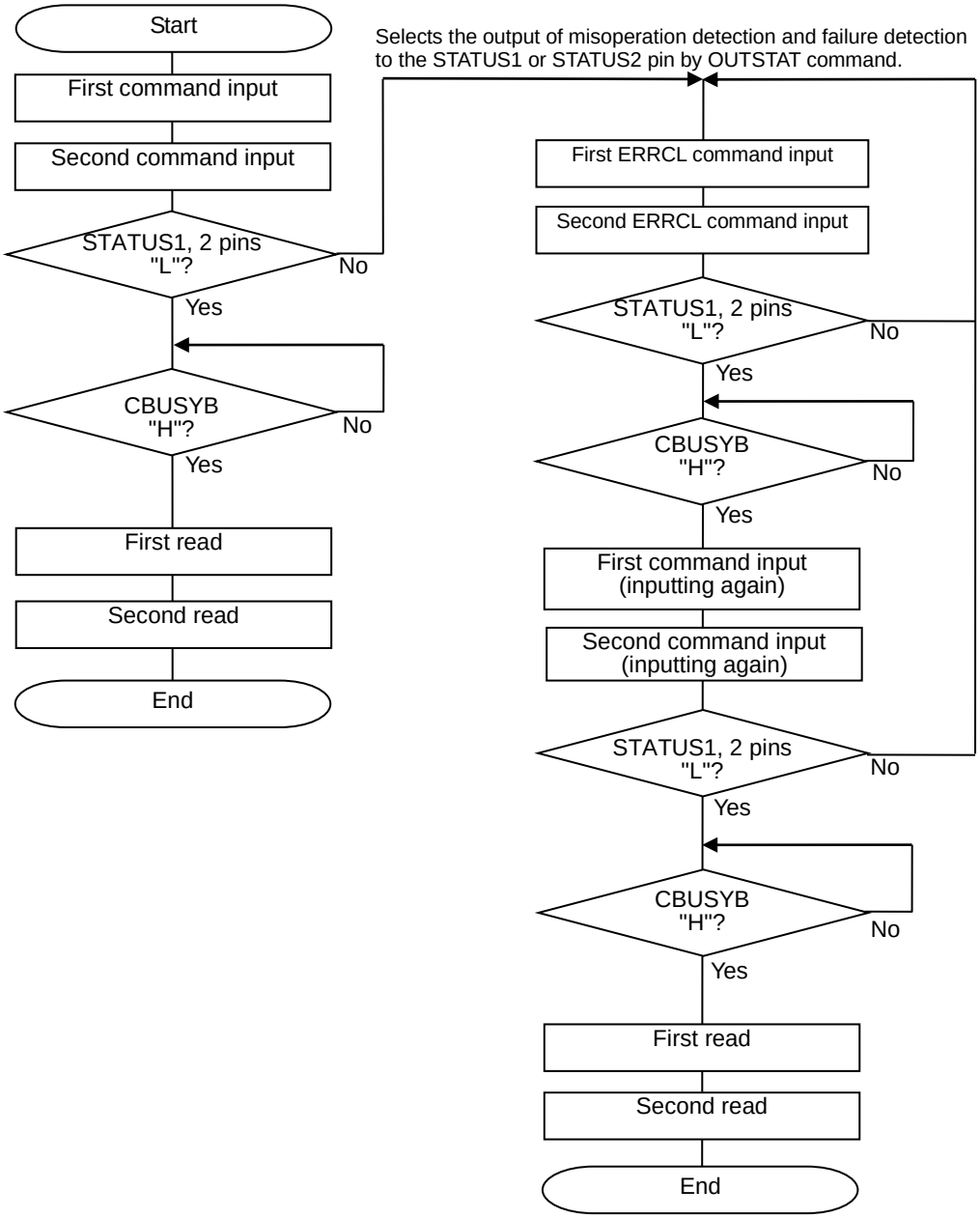
- 2-byte command input flow in two-times input mode



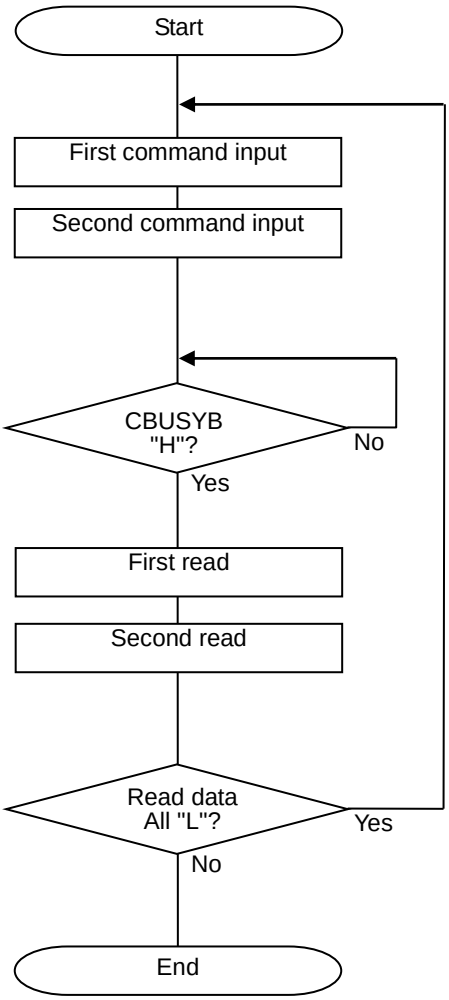
- 3-byte command input flow in two-times input mode



- Read flowchart in two-times input mode (Applies to RDSTAT, RDVER commands)



- Read flowchart in two-times input mode (Applies to RDERR command)



When the OUTSTAT command is used to select the misoperation detection and failure detection outputs and the STATUS1 or STATUS2 pin is "H", if all the read data is "L", the data cannot be read normally. Read the data again.

■ Peripheral circuit

- Handling of SG Pin

  The SG pin is the signal ground for the built-in speaker amplifier. Connect a capacitor between this pin and the SPGND to prevent noises.

Pin	Symbol	Recommended Constant
SG	C9	0.1µF±20%

- Handling of V_{DDL} Pin

  The V_{DDL} pin is a power supply for the internal circuits. Connect a capacitor across the DGND to prevent noises and power supply fluctuations. Please place it near the LSI on the user board.

Pin	Symbol	Recommended Constant
V_{DDL}	C8	1µF±20%

- Power wiring

  The power supply of this LSI is divided into the following three power supplies.
  - Digital power supply (DV_{DD}), digital GND (DGND)
  - Speaker amplifier power supply (SPV_{DD}), Speaker amplifier GND (SPGND)
  - Power supply for flash memory interface (IOV_{DD})

  These power supplies can be used independently. However, use it in the condition of $SPV_{DD} \geq DV_{DD}$.
  When using the same power supply, branch it from the root of the power supply for wiring.

- Bypass capacitor

  To improve noise-resistance, place the bypass capacitor close to the LSI on the user board, and shorten the wiring as short as possible without passing through the via.

Pin	Symbol	Recommended Constant
SPV_{DD}	C3	3.3µF±20%
SPV_{DD}	C4	0.1µF±20%
DV_{DD}	C5	3.3µF±20%
DV_{DD}	C6	0.1µF±20%
IOV_{DD}	C7	1µF±20%

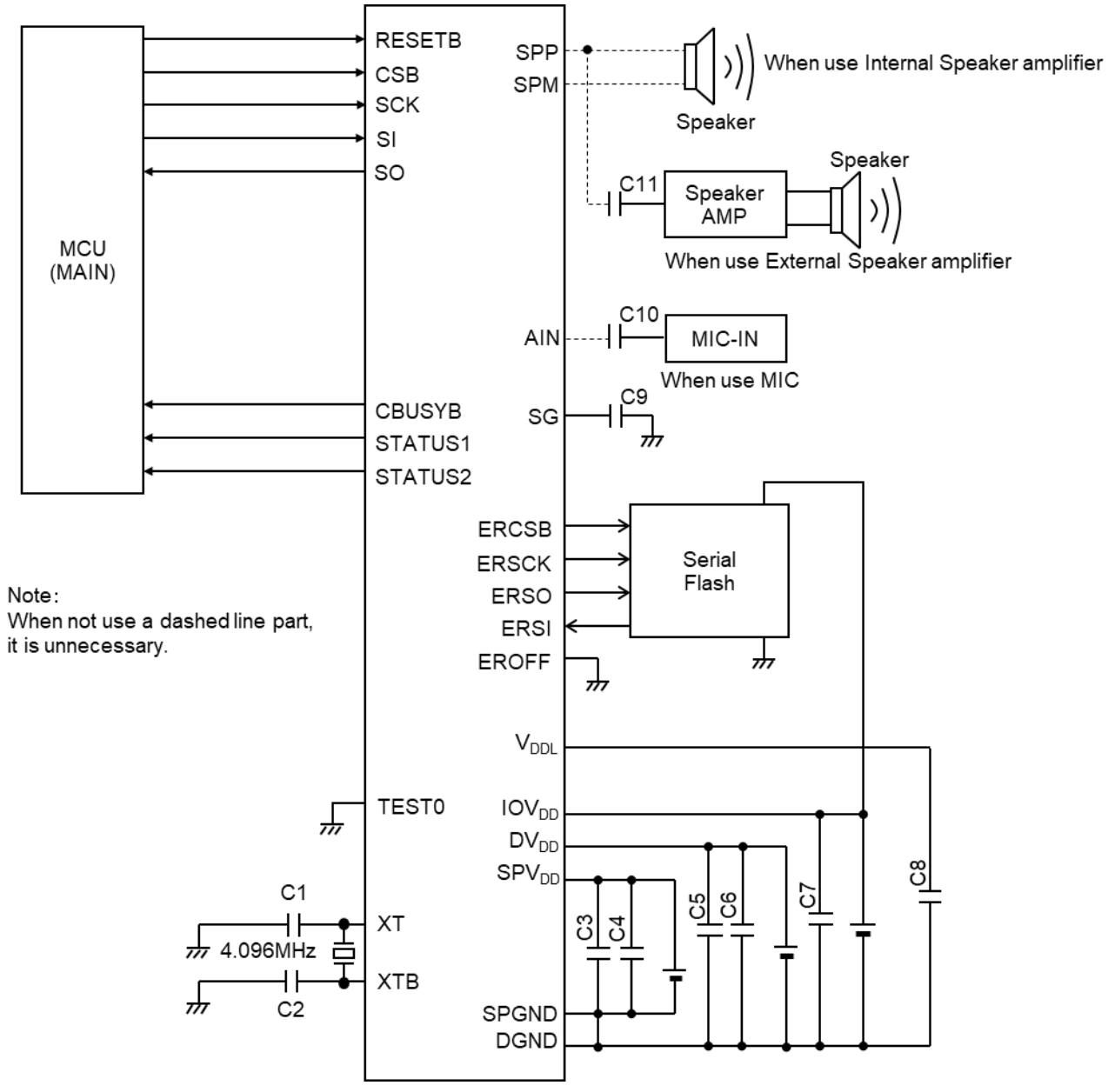
- Coupling capacitor

  Insert when analog input from AIN pin.
  Insert when using SPP pin as line amplifier output.

Pin	Symbol	Recommended Constant
AIN	C10	0.1µF±20%
SPP	C11	0.1µF±20%

■ Application Circuit

- synchronous serial interfaces



Please add necessary bypass capacitor to a power supply pin of the serial flash memory separately.
The power supply for the ERCSB, ERSCK, ERSO, ERSI and EROFF pins is IOV_{DD}.
If the crystal unit has a built-in capacitor, C1 and C2 are not needed.

■ Recommended ceramic resonator

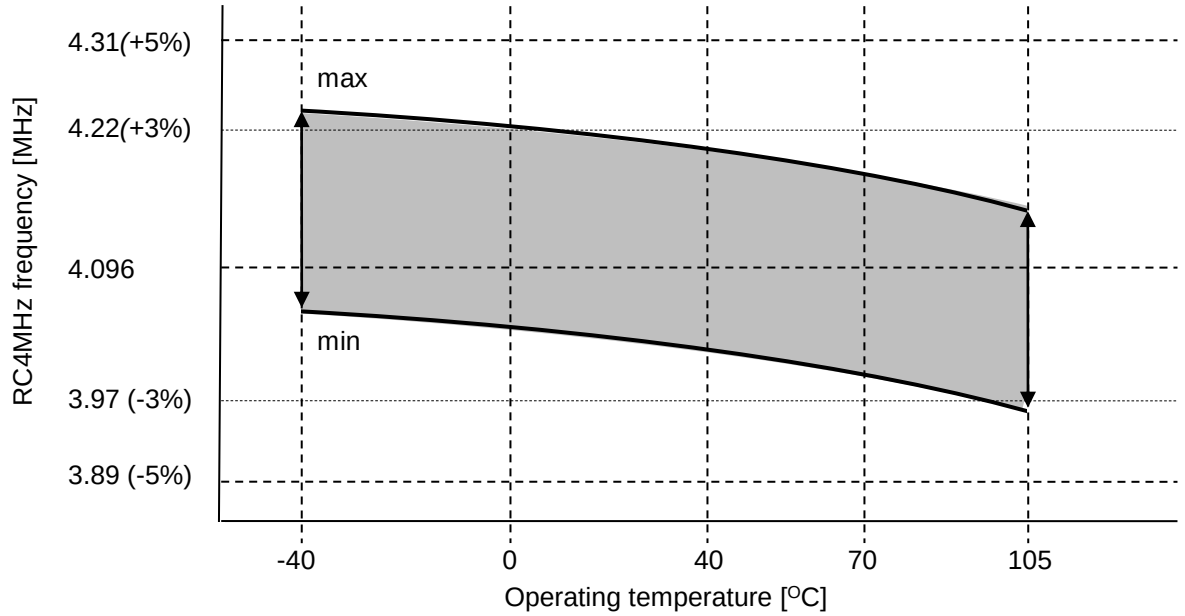
Recommended ceramic resonators are shown below.

- MURATA Corporation

Frequency [Hz]	Product Name	Built-in load capacity [pF]
4M	CSTCR4M00G55B-R0	39
4.096M	CSTCR4M09G55B-R0	

■ RC4MHz characteristic

RC4MHz characteristic is as follows.



This graph is for reference only and does not guarantee the electrical characteristic.

■ Limitation on the operation time (Playback operating time)

This LSI operating temperature is 85^{O}C (max). But the average ambient temperature at 1W playback (8ohm drive) for 10 years in the reliability design is Ta=65^{O}C. (max (the package heat resistance θja=31.58[^{O}C/W]))

When this LSI operates 1W playback (8ohm drive) consecutively, the product life changes by the package temperature rise by the consumption. This limitation does not matter in the state that a speaker amplifier does not play.

The factors to decide the operation time (playback operating time) are the average ambient temperature (Ta), playback Watts (at the speaker drive mode), the soldering area ratio, and so on. In addition, the limitation on the operation time changes by the heat designs of the board.

■ Package Heat Resistance Value (Reference Value) (θja)

The following table is the package heat resistance value θja (reference value).
This value changes the condition of the board (size, layer number, and so on).

< 32-pin TQFP>

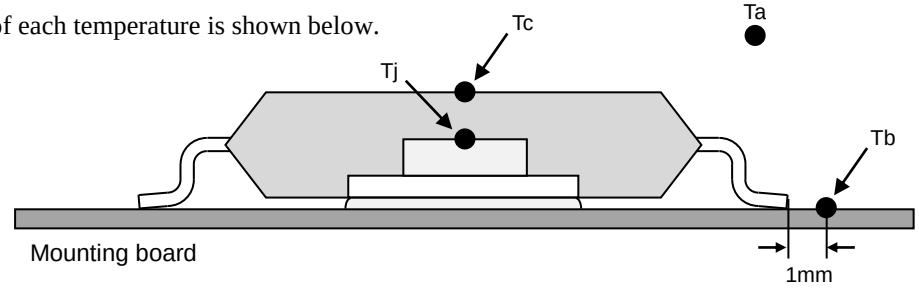
Board	θja	Ψjc	Ψjb	Condition
JEDEC 4layers*1 (W/L/t=76.2/114.5/1.6(mm))	31.58[^{O}C/W]	0.57[^{O}C/W]	11.64[^{O}C/W]	Air cooling condition: No wind (0m/s)
JEDEC 2layers*2 (W/L/t=76.2/114.5/1.6(mm))	37.77[^{O}C/W]	0.61[^{O}C/W]	12.43[^{O}C/W]	the soldering area ratio*3 : 100%

< 32-pin WQFN>

Board	θja	Ψjc	Ψjb	Condition
JEDEC 4layers*1 (W/L/t=76.2/114.5/1.6(mm))	32.86[^{O}C/W]	0.31[^{O}C/W]	7.65[^{O}C/W]	Air cooling condition: No wind (0m/s)
JEDEC 2layers*2 (W/L/t=76.2/114.5/1.6(mm))	44.01[^{O}C/W]	0.39[^{O}C/W]	8.39[^{O}C/W]	the soldering area ratio*3 : 100%

*1 : The wiring density : 1st layer(Top) 60% / 2nd layer 100% / 3rd layer 100% / 4th layer(Bottom) 60%.
*2 : The wiring density : 1st layer(Top) 60% / 2nd layer(Bottom) 100%.
*3 : The soldering area ratio is the ratio that the heat sink area of this LSI and a land pattern on the board are soldered. 100% mean that the heat sink area of this LSI is completely soldered to the land pattern on the board. About the land pattern on the board, be sure to refer to the next clause (Package Dimensions).

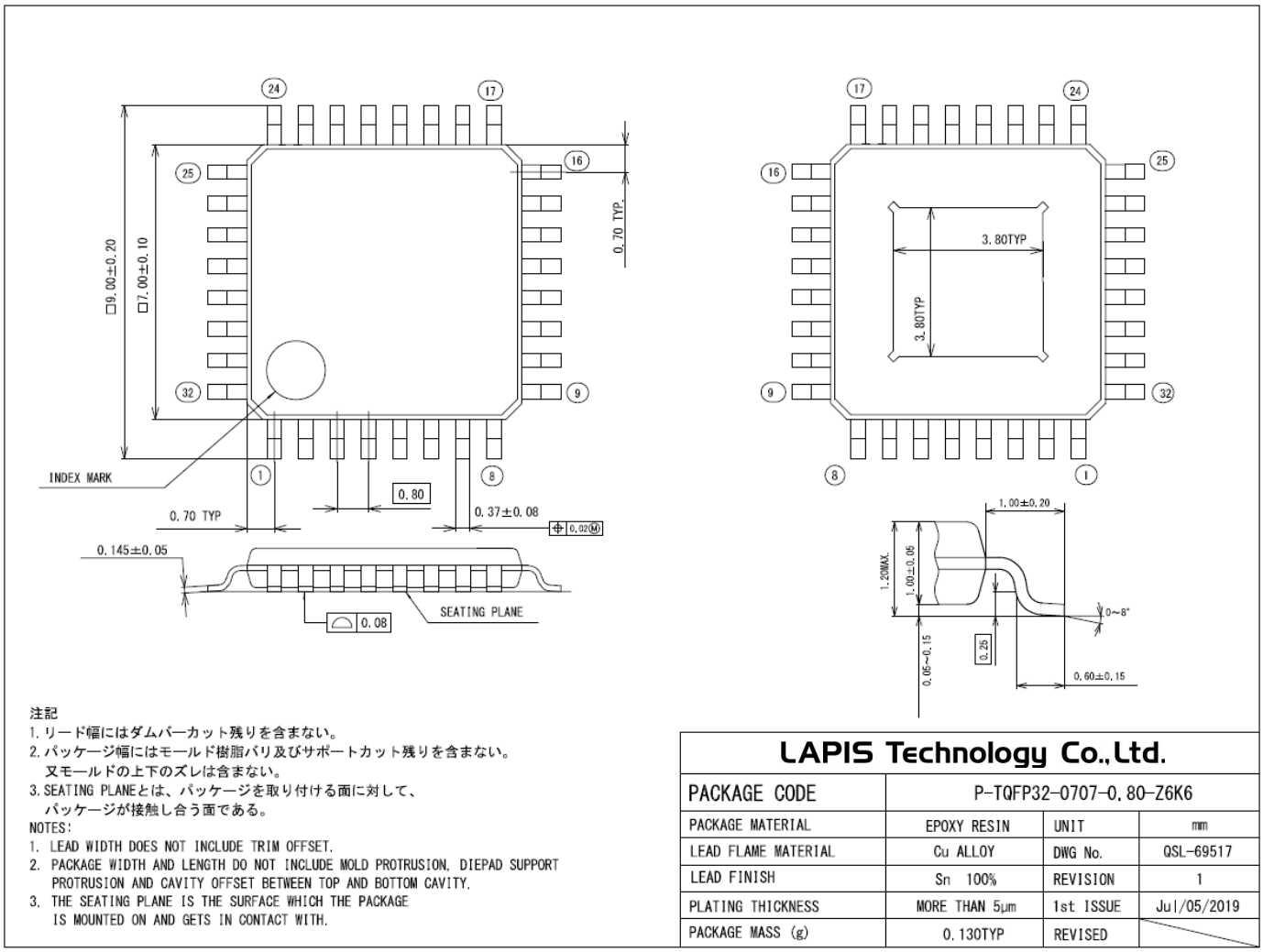
The definition of each temperature is shown below.



Take measures to dissipate heat on the mounting board so that the maximum junction temperature does not exceed 125 ^{O}C.

■ Package Dimensions

- ML22620TB



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
   又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
   パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

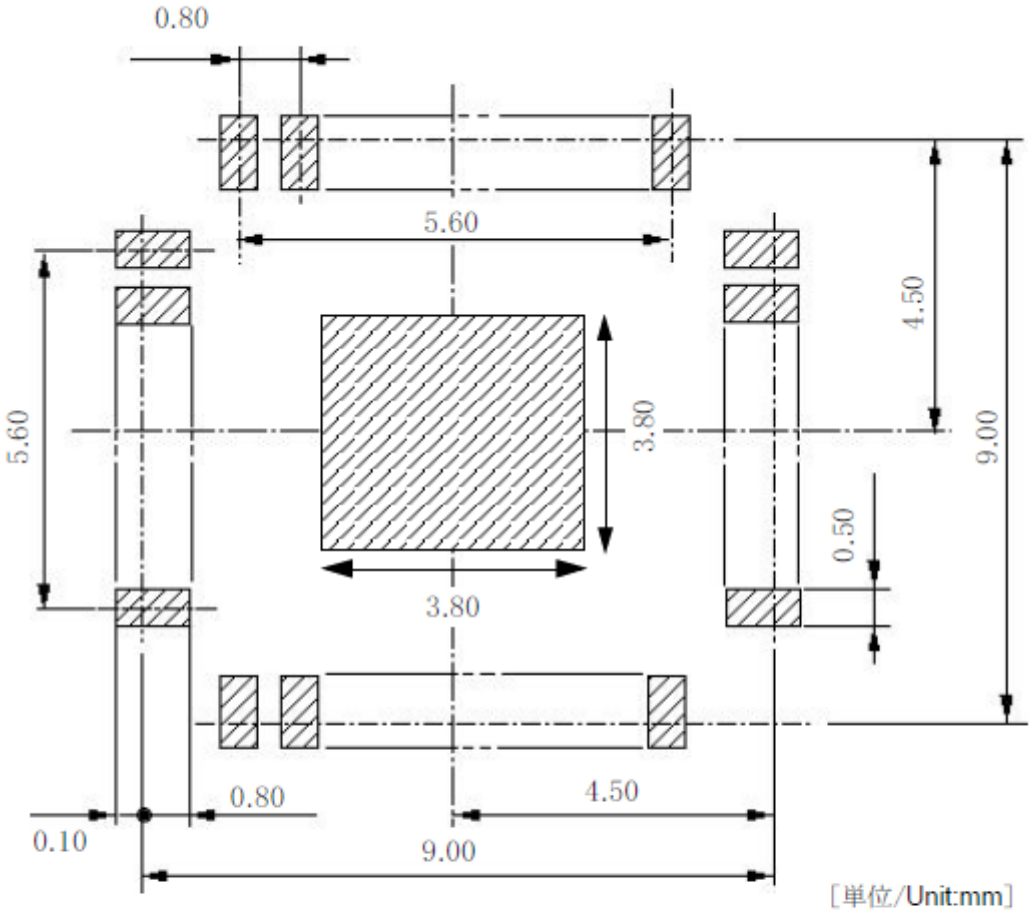
LAPIS Technology Co.,Ltd.			
PACKAGE CODE	P-TQFP32-0707-0.80-Z6K6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69517
LEAD FINISH	Sn 100%	REVISION	1
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/05/2019
PACKAGE MASS (g)	0.130TYP	REVISED	

Notes for heat sink type Package

This LSI adopts a heat sink type package to raise a radiation of heat characteristic. Design a land pattern on the board that corresponds to the exposed area of the LSI die pad, and Solder the exposed die pad to the board. The potential of the board connected to the exposed die pad should be GND or open. A diagram of the range of terminal presence on the board (reference data) is shown on the next page.

半田付け部端子存在範囲図

Mounting area for package lead soldering to PC boards



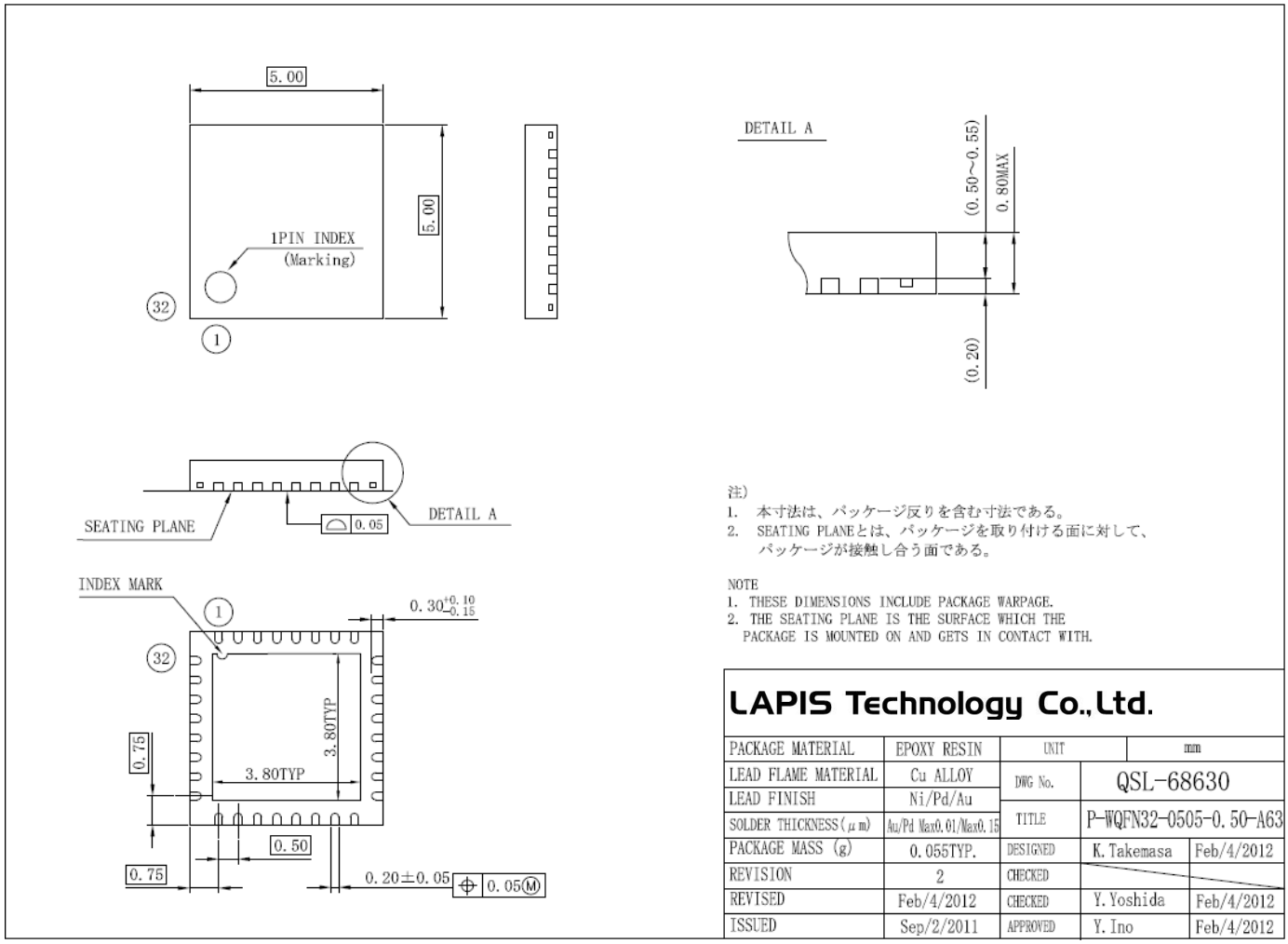
実装基板のフットパターンの設計の際には、実装の容易さ、接続の信頼性、配線の引き回し、半田ブリッジ発生のないことなどを十分考慮してください。

フットパターンの最適な設計は基板材質、使用する半田ペースト種類、厚み、半田付け方法などによって変わってきます。従って、本パッケージの端子の存在し得る範囲を「半田付け部端子存在範囲図」として示しますので、フットパターン設計の参考資料としてください。

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts,reliability, wiring,and elimination of solder bridges.

The optimum design for the foot pattern varies with the materials of the substrate,the sort and thickness of used soldering paste,and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering to PC boards.

- ML22620GD

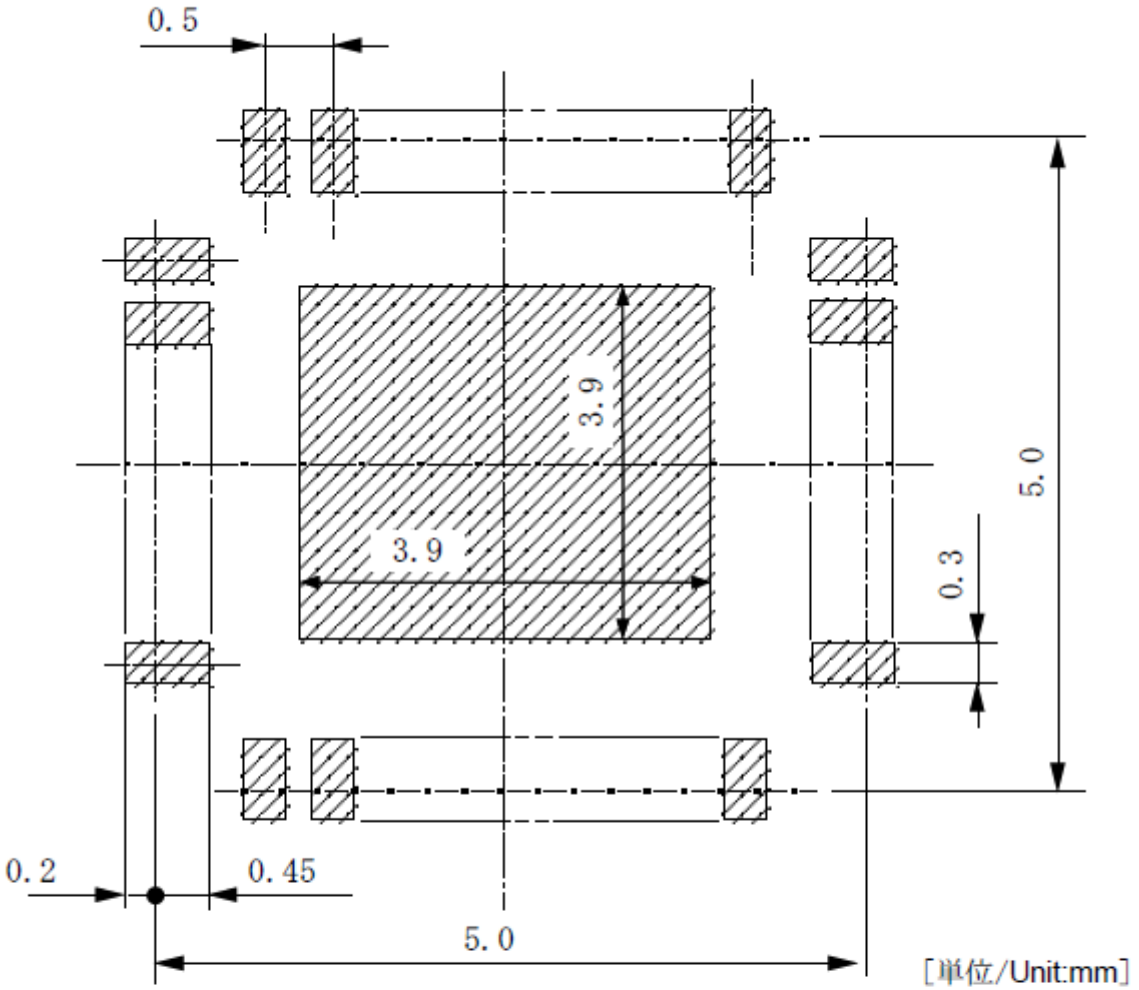


Notes for heat sink type Package

This LSI adopts a heat sink type package to raise a radiation of heat characteristic. Be sure to design the land pattern corresponding to the heat sink area of the LSI on a board, and solder each other. The heat sink area of the LSI solder open or GND on the board.

半田付け部端子存在範囲図

Mounting area for package lead soldering to PC boards



実装基板のフットパターンの設計の際には、実装の容易さ、接続の信頼性、配線の引き回し、半田ブリッジ発生のないことなどを十分考慮してください。

フットパターンの最適な設計は基板材質、使用する半田ペースト種類、厚み、半田付け方法などによって変わってきます。従って、本パッケージの端子の存在し得る範囲を「半田付け部端子存在範囲図」として示しますので、フットパターン設計の参考資料としてください。

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■ Differences from Existing Speech Synthesis LSIs (ML22420)

Parameter		ML22420	ML22620
MCU command interface		Clock synchronous serial	←
Clock frequency		4.096MHz (Built-in crystal oscillation circuit)	4.096MHz (Crystal oscillation circuit/built-in RC Oscillation)
Memory capacity	External	Up to 128Mbits	←
Flash memory rewrite function		-	MCU command interface (Clock synchronous serial)*1
Sound function	Speech synthesis algorithm	4bit ADPCM2 8-bit non-linear PCM 8bit PCM 16-bit PCM	HQ-ADPCM 4bit ADPCM2 8-bit non-linear PCM 8bit straight PCM 16-bit straight PCM
	Sampling frequency (kHz)	6.4/12.8/25.6 4.0/8.0/16.0/32.0 5.3/10.7/21.3 12.0/24.0/48.0	6.4/12.8/25.6 8.0/16.0/32.0 10.7/21.3 11.025/22.05/44.1 12.0/24.0/48.0
	Simultaneous sounding function (Mixing-function)	4 channels	←
	Maximum number of phrases	1024@1BANK	4096
	BANK	4	-
	Edit ROM function	Yes	←
	Silence insertion function	20ms to 1024ms (4ms step)	←
	Repeat function	Yes	←
Low-pass filter		FIR type interpolation filter	←
D/A converter		Voltage type 16-bit	←
Speaker amplifier		Class AB 0.7W@8Ω (SPV_{DD}=5V)	Class AB/D 1.0W@8Ω (SPV_{DD}=5V)
Volume adjustment function	Digital	32 levels	128 levels
	Analog	50 levels	16 levels
	Fade function	-	Yes
External analog input		Yes	←
Failure detection function	Clock error detection	-	Yes
	Thermal detection	-	Yes
	Speaker pin ground fault detection *2	-	Yes
	Speaker pin short detection *2	-	Yes
	Speaker disconnection detection	-	Yes
Power-supply voltage		DV_{DD}=SPV_{DD}=2.7 to 5.5V	DV_{DD}=2.7 to 5.5V SPV_{DD} ≥DV_{DD} IOV_{DD}=2.7V to 5.5V
Operating temperature		-40 to 85°C	←
Package		30-pin SSOP	32-pin TQFP 32-pin WQFN

*1 Controlling EROFF pin can prohibit the serial flash memory interface and can rewrite the serial flash memory by connecting flash wrighter.

*2 The ground fault detection and short-circuit detection functions can be used when the SPV_{DD} is 4.5V or higher.

It becomes command-compatible with ML22420 by using the following command setting.

Command name	Bit name	Bit value
PUP	WCM	0
AMODE	HPF	0

■ Speech LSI Utility Setting Items

Set the following items on the Speech LSI Utility.

Item	Description
Protection code for serial flash memory access	Set any 8-bit data. ・0x69: Flash memory cannot be accessed by the FDIRECT command. ・Other than 0x69: Accessing the flash memory is enabled when the protection unlock data entered by the FDIRECT command matches the data.
Master clock selection	Select master clock(Source clock oscillation). ・RC (RC oscillation) ・Xtal (Crystal or ceramic resonator)
Master clock frequency	Set the master clock frequency to F_{OSC}. ・4.096 : 4.096MHz setting ・4.000 : 4.000MHz setting
Number of phrases used	Select the number of phrases from the following. ・4096 ・3072 ・2048 ・1024
Sound ROM information	Set any 8-bit data. Read by RDVER command.
Class D amplifier output format	Output format selection. ・Half-wave mode Full wave mode is not supported.
WDT counter, RST counter WDTERR or RSTERR processing at overflow	Select the processing to be performed when an overflow occurs. ・Hold current state ・Transition to the state after PUP command input
WDT counter, RST counter WDTERR or RSTERR overflow time	Select the overflow time from the following. ・125ms ・500ms ・2s ・4s

Refer to the Speech LSI Utility User's Manual for more information.

■ Check lists

This check list has notes to frequently overlooked or misunderstood hardware features of the LSI. Check each note listed up chapter by chapter while coding the program or evaluating it using the LSI.

■Feature

[ ] *1 The operating time of the speaker amplifier may be limited depending on the average ambient temperature (Ta) used.

■Pin Description

[ ] (TEST1 pin) Leave open.
[ ] (EROFF pin) Set this pin to "L" during playback operation using serial flash memory.
[ ] (EROFF pin) Set this bit to "H" for onboard rewriting.
[ ] (IOV_{DD} pin) Connect a bypass capacitor between this pin and the DGND pin.
[ ] (XTB pin) When using a resonator, connect it as close as possible.
[ ] (XTB pin) Leave it open when not in use.
[ ] (XT pin) To use an external clock, input from this pin. Delete the capacitor when a crystal or ceramic resonator is connected.
[ ] (XT pin) When using a resonator, connect it as close as possible.
[ ] (XT pin) Leave it open when not in use.
[ ] (DV_{DD} pin) Connect a bypass capacitor between this pin and the DGND pin.
[ ] (V_{DDL} pin) Connect a capacitor between this pin and DGND pin as close as possible.
[ ] (SG pin) Connect a capacitor between this pin and SPGND pin.
[ ] (SPV_{DD} pin) Connect a bypass capacitor between this pin and the SPGND pin.
[ ] (RESETB pin) At power-on, input an "L" level to this pin. After the power supply voltage stabilizes, set this pin to an "H" level.
[ ] (TEST0 pin) Fix to the DGND.
[ ] (CBUSYB pin) Be sure to input a command with this pin at an "H" level.
[ ] (N.C. pin) Unused pin. Leave open.

■Termination of Unused Pins

[ ] Confirm the recommended termination of unused pins in this chapter.

■Electrical characteristics

●Recommended operating conditions

[ ] *1 Be sure to $SPV_{DD}>=DV_{DD}$.

■Function description

●Mixing function

◆ Waveform clamp precautions for mixing

[ ] If the clamp is known to be generated in advance, adjust the volume of each channel by CVOL command.

◆ Class D amplifier precaution on mixing

[ ] Short detection of SPP pin and SPM pin always operates while using the class D amplifier. If the volume of CVOL command is adjusted incorrectly and it it is played back in the clamped state, the short detection circuit is determaine that a short has occurred.When using class D amplifier, enable short detection of SPP pin and SPM pin by SAFE command and check the short detection error (SPDERR).

◆ Different sampling frequency mixing algorithm

[ ] It is not possible to perform channel mixing by a different sampling frequency group.Note that when channel synthesis is performed on a sampling frequency group other than the selected sampling frequency group, playback will be faster or slower.

●Misoperation detection and failure detection functions

◆ SPP pin and SPM pin short detection

[ ] After inputting SAFE command, start the analog power-up operation by AMODE command within 10ms.

◆ Flash memory error detection

[ ] If the error bit (ROMERR) is set to "1" after the PUP command and before the PLAY command or START command starts playback, this LSI may have error at the time of start. In such cases, initialize this LSI by moving the LSI to the power-down mode by resetting the LSI by the RESETB pin or by using PDWN command.

◆ Detects the stop of clock input from a crystal resonator or ceramic resonator

[ ] If the RDERR command (first byte) is inputted before the crystal or ceramic resonator stops and switches to RC oscillation (about 500us), the CBUSYB pin will remain "L". Therefore, read the command after the CBUSYB pin becomes "H".

[ ] When the crystal resonator or the ceramic resonator stops and switches to RC oscillation, playback may become abnormal. Therefore, after confirming that the error bit (OSCERR) is "1", enter STOP command to stop playback.

●Serial flash memory rewrite function

[ ] When rewriting the serial flash memory using the CSB, SCK, SI, and SO pins, which are clock synchronous serial interfaces of the MCU command interface, set the SCK pin to 'H' level when the CSB pin falls, and data should be taken in on the rising edge of the SCK pin clock and output data on the falling edge.

■Timing chart

●Power-on timing

[ ] Start up in the order of DV_{DD}, SPV_{DD} and IOV_{DD} or DV_{DD}, IOV_{DD} and SPV_{DD}.

[ ] Be sure to input "L" to the RESETB pin before inputting the first command after power-on.

[ ] Be sure to enter "L" at the RESETB pin when the DV_{DD} is below the (recommended) operating voltage range.

●Power-off timing

[ ] Shut down in the order of IOV_{DD}, SPV_{DD}, and DV_{DD} or SPV_{DD}, IOV_{DD}, and DV_{DD}.

[ ] Shut down each power supply after changing to the power down status with PDWN commands.

●Change volume timing by AVOL command

[ ] Speaker amplifier volume setting by AVOL commands is valid only when Class AB speaker amplifier is used.
When a Class D speaker amplifier is used, the setting value is ignored and +0.0dB is selected.

●Continuous playback timing by PLAY command

[ ] When making continuous playbacks, input the PLAY command for the next phrases within the specified time period (tcm) after the NCR of the corresponding channel changes to "H" level.

[ ] When the playback is not continuous, input the PLAY command for the next phrases after confirming the playback is completed by RDSTAT command and etc.

●Continuous playback timing by START command

[ ] When making continuous playbacks, send the START command for the next phrases within the specified time period (tcm) after the NCR of the corresponding channel changes to "H" level.

[ ] When the playback is not continuous, input the START command for the next phrases after confirming the playback is completed by RDSTAT command, etc.

●Continuous playback timing by MUON command

[ ] When making continuous playbacks, input the MUON/PLAY/START command for the next phrases within 10ms (tcm) after the NCR of the corresponding channel changes to "H" level.When the playback is not continuous, input the MUON/PLAY/START command for the next phrases after confirming the playback is completed by RDSTAT command and etc.

●Repeat playback setting/release timing by SLOOP/CLOOP command

[ ] The SLOOP command is valid only during playback. After the PLAY command is input, input the SLOOP command within the specified period (tcm) after the NCR of the corresponding channel becomes "H" level.

■Command

●Command list

[ ] Do not enter command that is not described in this manual. Enter the command with the CBUSYB "H".

●Description of Command Functions

◆ AMODE command

[ ] To perform power-down under a setting condition that differs from the power-up condition of the analog unit, set the AMODE command to set the power-down condition again.

[ ] To power up the analog part, set the CVOL command to 00h (initial value) and then enter the AMODE command.

[ ] When using analog mixing from the AIN pin, set DAMP = "0" (Class AB amplifier is used). In this LSI, select DAMP = "0" (Class AB amplifier is used).

[ ] Input the sound signals to the AIN pin after CBUSYB pin becomes "H" by the AMODE command.

[ ] When using a Class D amplifier with speaker amplifier outputs, set it to the power-up state (AEN1/AEN0= "01") or the power-down state (AEN1/AEN0= "00"). If DAMP = "1" is selected, do not set AEN1= "1".

◆ AVOL command

[ ] AV5-AV2=1h and 2h are prohibited.

◆ FDIRECT command

[ ] The FDIRECT command controls accesses to the flash memory using the clock-synchronous serial interface.Input the command after inputting the PUP command.

[ ] To cancel the flash memory access mode, insert a reset (RESETB = "L") and conduct initialization or turn off the power supply.

◆ START command

[ ] Be sure to specify one of the channels for the channel setting (CH0-CH3). Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

◆ STOP command

[ ] The STOP command can be input regardless of the status of the NCR during playback operation. However, following the elapse of CBUSYB "L" level output time 3 (tCB3), input the next command after confirming that the BUSYB signal becomes "H". If the BUSYB signal does not become "H", enter the STOP command again.

[ ] Be sure to specify one of the channels for the channel setting (CH0-CH3). Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

◆ MUON command

[ ] Set the silence setting (M7-M0) to 04h or more (tmu>=20ms).

[ ] Be sure to specify one of the channels for the channel setting (CH0-CH3). Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

◆ SLOOP command

[ ] Be sure to specify one of the channels for the channel setting (CH0-CH3). Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

◆ CLOOP command

[ ] Be sure to specify one of the channels for the channel setting (CH0-CH3).Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

◆ CVOL command

[ ] Be sure to specify one of the channels for the channel setting (CH0-CH3). When multiple channels are specified, the volume of the specified channels is set. Do not input it to "0" (all “0”) with specifying nothing. If it is input with specifying nothing (all "0"), the command is ignored.

◆ RDSTAT commnad

[ ] When reading the status of the second byte after command input, set the SI pin to "L".

◆ RDVER command

[ ] When reading the status of the second byte after command input, set the SI pin to "L".

◆ RDERR command

[ ] When reading the status of the second byte after command input, set the SI pin to "L".

[ ] If the outputs of misoperation detection and failure detection are selected by OUTSTAT command, and the read data is all "L" even though STATUS1 or STATUS2 pin is "H", the read data cannot be read normally. Be sure to read it again.

◆SAFE command

[ ] The initial value is the operation stop state ("0"). When this bit is set to "1", operation starts.

[ ] *1 Do not set WDTEN and RSTEN to "1" at the same time. If these bits are set to "1" at the same time, only the RSTEN bit is set to "1".

■Peripheral circuit

●Handling of SG Pin／●Handling of V_{DDL} Pin／●Power wiring／●Bypass capacitor／●Coupling capacitor

[ ] Confirm the recommended values and precautions in this chapter.

■Package Dimensions

[ ] Confirm “Notes for heat sink type Package” and “Notes for Mounting the Surface Mount Type Package” in this chapter.

■Speech LSI Utility Setting Items

[ ] Confirm setting items of “Speech LSI Utility” in this chapter.

■ Revision history

Document No.	Date	Page		Description
		Previous edition	Current edition	
FEDL22620-01	Apr 24, 2020	-	-	Formal 1st edition.
FEDL22620-02	Jul 17, 2020	2	2	Added "DV_{DD}, SPV_{DD} and IOV_{DD} can be set independently. ($SPV_{DD} \geq DV_{DD}$)" to the description of power-supply voltage.
		11	11	Added "*2" to the standard value of I_{DDO} and I_{DDS} of DC characteristics.
		19	19	Added definition of compression rate.
		— 84	23 85	Added class D amplifier precaution on mixing.
		25	26	Changed description of command error detection. (Not a change in product specijications.)
		29	30	Changed description of watchdog timer overflow detection. (Not a change in product specijications.)
		31	32	Changed description of RST counter overflow detection. (Not a change in product specijications.)
		34	35	Added a method to return from flash memory access mode to normal mode.
		37	38	Changed t_{EFHL} and t_{EFLH} of Serial flash memory interface timing.
		61	62	Changed description of DAMP bit of AMODE command. (Not a change in product specijications.)
		62	63	Changed description of POP bit of AMODE command. (Not a change in product specijications.)
		62	63	Changed description of table of AEN1, AEN0 and POP bit, of AMODE command. (Not a change in product specijications.)
		84	85	Changed description of OSCEN bit of SAFE command. (Not a change in product specijications.)
		101	102	Added attention of voltage setting of SPV_{DD} and DV_{DD} for power wiring.
		101	102	Added C11 to the coupling capacitor.
		103	104	Changed notation of recommended ceramic resonator. (Not a recommended product change.)
		—	112	Added class D amplifier precaution on mixing in the check lists.
FEDL22620-03	Oct 1, 2020	11	11	Addition of terminals to V_{OH3} (Before change) ERSO (After change) ERCSB / ERSCK / ERSO
		11	-	I_{IH4} deleted
		11	11	Change current consumption I_{DDO} value during playback operation (Before change) Max 45mA (After change) Typ 25mA,Max 45mA

Document No.	Date	Page		Description
		Previous edition	Current edition	
FEDL22620-03	Oct 1, 2020	13	13	When AMODE command is input CBUSYB "L" level output time t_{PUPA2} value change (Before change) min 72ms,typ 74ms,max 76ms (After change) min 71ms,typ 73ms,max 75ms
		13	13	When AMODE command is input CBUSYB "L" level output time t_{PUPA3} value change (Before change) min 32ms,typ 34ms,max 36ms (After change) min 31ms,typ 33ms,max 35ms
		13	13	When AMODE command is input CBUSYB "L" level output time t_{PDA1} value change (Before change) min 106ms,typ 108ms,max 110ms (After change) min 100ms,typ 102ms,max 104ms
		13	13	When AMODE command is input CBUSYB "L" level output time t_{PDA2} value change (Before change) min 143ms,typ 145ms,max 147ms (After change) min 142ms,typ 144ms,max 146ms
		13	13	When AMODE command is input CBUSYB "L" level output time t_{PDA3} value change (Before change) min 103ms,typ 105ms,max 107ms (After change) min 102ms,typ 104ms,max 106ms
FEDL22620-04	Jan 7, 2021	4	4	Added attention of ERCSB,ERSCK and ERSO output intial condition.
		14	14	Added t_{DOH} to the AC Characteristics (Clock Synchronous Serial Interface).
		17	17	Changed Clock Synchronous Serial Interface timing wave form.
		39	39	Changed Clock Synchronous Serial Interface timing wave form.
		62	62	Changed description of power down timming with POP noise noise suppression. (Not a change in product specijications.)
FEDL22620-05	Jan 14, 2022	2	2	Added " 32-pin WQFN (5mm x 5mm, 0.5mm pitch)" to Package Added "ML22620GD (32-pin WQFN)" to Ordered Part Name
		-	4	Added "ML22620GD (32-pin WQFN)" to Pin Configuration
		8	9	Classification F I/O Equivalent Circuit change (Before change) Input/Output (After change) Output
		8	9	Classification G I/O Equivalent Circuit change (Before change) Input/Output (After change) Output
		8	9	Classification H I/O Equivalent Circuit change (Before change) Input/Output (After change) Input
		12	13	RC4MHz Oscillation frequency Ta = -40 ~ + 85 ℃ Conditional characteristics added

Document No.	Date	Page		Description
		Previous edition	Current edition	
FEDL22620-05	Jan 14, 2022	34	35	Change the timing chart when the OSCEN bit of the SAFE command continues to be "1" (Before change) After ERRCL, when oscillation is stopped, the STATUSn pin and OSCERR maintain "L". (After change) After ERRCL, when oscillation is stopped, the STATUSn pin and OSCERR become "H".
		103	104	Added explanation about capacitors for crystal oscillators
		105	106	32-pin WQFN added to package thermal resistance
		-	109,110	Added "ML22620GD" to Package Dimensions
		108	111	Added " 32-pin WQFN " to Package
FEDL22620-06	Jul 10, 2023	107	107	(Before change) Be sure to design the land pattern corresponding to the heat sink area of the LSI on a board, and solder each other. The heat sink area of the LSI solder open or GND on the board. (After change) Design a land pattern on the board that corresponds to the exposed area of the LSI die pad, and Solder the exposed die pad to the board. The potential of the board connected to the exposed die pad should be GND or open. A diagram of the range of terminal presence on the board (reference data) is shown on the next page.
FEDL22620-07	Feb 9, 2024	-	3	Added application information.
		2	3	Changed shipping form to table format.
		122	122	Revised the Note.
FEDL22620-08	Mar 27, 2025	37	37	Added the precaution on the serial flash memory rewrite function.
		116	116	Added the precaution on the serial flash memory rewrite function in the check lists.
		122	-	Revised the Notice in the last page.

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