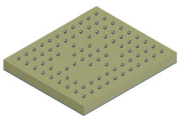
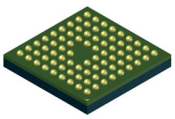
Audio Processor for Digital Hearing Aids and Hearables

EZAIRO 8300



WLCSP87
CASE 567ZN



VFBGA78
CASE 138AW

Introduction

Ezairo® 8300 includes six programmable or semi−programmable processing cores, providing a high degree of parallelism and flexibility:

- The CFX is an open−programmable dual−Harvard 24 bits digital signal processor (DSP) providing support for any type of audio signal processing
- The Arm® Cortex®−M3 processor is a 32−bit RISC processor providing support for general processing and interfacing to external components
- The HEAR configurable accelerator core is optimized for pre−programmed functions that are frequently needed in audio signal processing
- The Filter Engine allows time domain filtering and supports an ultra−low−delay audio path
- The LPDSP32 is an open−programmable dual−Harvard 32−bit DSP
- The Neural Network Accelerator that allows the Ezairo 8300 to perform neural network computations in a highly efficient and flexible way.

Ezairo 8300 includes 4 ADCs with signal detection mode and 2 direct digital output drivers, with high quality and ultra−low power performances. Ezairo 8300 also includes peripherals and interfaces needed to make it a complete hardware platform, when combined with non−volatile memory and wireless transceivers.

MARKING DIAGRAMS



WLCSP87



VFBGA78

o = Pin 1 indicator
XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
ZZ = Wafer Number
CCC = Country of Origin
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
E8300−101WC78−ABG	WLCSP	5000 / Tape & Reel
E8300−101B78−ABG	VFBGA	
E8300−101WC78−BBG	WLCSP	100 / Tape & Reel For prototyping only
E8300−101B78−BBG	VFBGA	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Key Features

- **High Performance:** Best in class MIPS/mW.
- **Programmable Flexibility:** the open−programmable DSP−based system can be customized to the specific signal processing needs of manufacturers. Algorithms and features can be modified or completely new concepts implemented without having to modify the chip.
- **Highly−integrated SoC:** the six−core architecture includes a CFX DSP, an Arm Cortex−M3 Processor, a HEAR Configurable Accelerator, a programmable Filter Engine, a LPDSP 32 DSP and a Neural Network Accelerator. The system also includes an efficient input/output controller (IOC), system memories, input and output stages along with a full complement of peripherals and interfaces.
- **CFX DSP:** a highly cycle−efficient, programmable core that uses a 24−bit fixed−point, dual−MAC, dual−Harvard architecture. The CFX can be used as the master of the whole Ezairo 8300 SoC.
- **Arm Cortex−M3 Processor:** a complete subsystem that can be used as the master of the whole Ezairo 8300 SoC.
- **HEAR Configurable Accelerator:** a highly optimized signal processing engine designed to perform common signal processing operations and complex standard filterbanks.
- **Programmable Filter Engine:** a filtering system that allows applying a various range of pre− or post−processing filtering, such as IIR, FIR and biquad filters.
- **LPDSP32:** a highly cycle−efficient, programmable core that uses a 32−bit fixed−point, dual−MAC, dual−Harvard architecture.
- **Neural Network Accelerator (NNA):** a configurable hardware accelerator dedicated to support neural networks with high energy efficiency.
- **Selectable System Clock Speeds:** from 2.56 MHz up to 61.44 MHz, with clock throttling capabilities to optimize the computing performance versus power consumption ratio.
- **Adaptive Voltage Scaling:** automatically adjusts the digital supply voltage (VDDC) level using a critical path speed measurement block. This feature allows to optimize the SoC's power consumption in all situations.
- **Ultra−low Delay path:** the programmable Filter Engine supports an ultra−low−delay audio path of min 10.4 μs (analog input to analog output) for features such as active noise cancellation.
- **Ultra−low Power Consumption:** <0.7 mA @ 15.24 MHz system clock (CFX 97%, Arm Cortex−M3 processor 40%, HEAR 77%, FENG 9%, 2 ADC @ 20 kHz, 1 OD, 1 LSAD)
- **High fidelity audio system:** 108 dB system dynamic range, up to 64 KHz of sampling frequency
- **Output drivers:** capable of driving multiple types of speakers.
- **Versatile Memory Architecture:** a total of 1433 kB of memory, shared between the six programmable or semi−programmable cores.
- **Data Security:** sensitive program data can be encrypted for storage in external NVM to prevent unauthorized parties from gaining access to proprietary algorithm and intellectual property.
- **Multiple Audio Input Sources:** four analog input channels (AI0 to AI3) that can be used simultaneously for omni−directional and directional microphones, telecoils, bone conducting microphones, an input from a remote control interface, or a direct audio input.
- **Signal Detection Mode:** ultra−low−power detection system for signals on any analog inputs.
- **High Throughput Communication Interface:** fast I^2C−based and SWJ−DP interfaces for quick download, debugging and general communication.
- **Highly Configurable Interfaces:** two PCM interfaces, three I^2C interfaces, two I^3C interfaces, two SPI interfaces, a UART interface, an eMMC interface with custom interface buffering, up to 36 GPIOs and 8 LSAD inputs.
- **Asynchronous Sample Rate Converter (ASRC):** provides a mean of synchronizing the audio sample rate between an external radio chip and the Ezairo 8300.
- **Two Audio Sink Clock Counters:** Can be used to measure the timing of the frame periods of an external radio relative to the internal audio sampling rate.
- **Fitting Support:** support for Microcard, HI−PRO 2, HI−PRO USB, QuickCom, and NOAHlink, including NOAHlink's audio streaming feature.
- **Integrated Development Environment (IDE):** a graphical user interface with the capabilities to edit, build and debug applications. It is the main programming interface for the Software Development Kit (SDK).
- **Complete C−development tool chain for the CFX and the LPDSP32.** Includes a C−compiler, an instruction set simulator, an assembler/disassembler, a linker and the IDE debugger integrated in the Ezairo 8300 SDK.
- **Sample Code:** The SDK includes several sample applications and libraries to demonstrate key features of Ezairo 8300. The libraries are typically provided in compiled form with source code also available.
- **Pb−Free Device**

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Typ	Max	Unit	Notes
VBAT	–	–	1.98	V	Power supply voltage
VBATOD	–	–	1.98	V	Output driver power supply voltage
VDDO1/2/3/4	–	–	1.98	V	I/O supply voltage
VSSA	0	–	–	V	Analog ground
VSSOD	0	–	–	V	Output driver ground
VSSC	0	–	–	V	Digital ground
VSSO	0	–	–	V	I/O ground
Vin	VSSO−0.1	–	VDDO+0.3	V	Digital input pin voltage
	−0.1	–	1.98	V	Digital input pin voltage
Toperation	0	25	50	°C	Operational temperature
Tfunctional	−40	25	85	°C	Extended op. temperature (Note 1)
Tstorage	−40	–	125	°C	Storage temperature
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V) The device in VFBGA package meets 250 V CDM level, JESD22−C101.					

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The IC is functional in the extended temperature range, however some parameters may not meet the specifications. E.g. bandgap voltage, oscillator frequency, ADC noise...

Table 2. OVERALL OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit	Notes
VBAT	0.9	1.25	1.98	V	Supply voltage, measured at the VBAT pin (Note 2)
VBATOD	0.9	1.25	1.98	V	Output driver supply voltage (Note 3)
VDDO1/2/3/4	0.9	1.25	1.98	V	I/O voltage (Note 4)
System clock	–	15.36	61.44	MHz	System clock frequency
VDDC retention	0.50	0.53 (Note 5)	–	V	Digital supply voltage, when memories are in retention mode
VDDC limit	0.50	0.51 (Note 5)	–	V	Digital supply voltage limit for adaptive voltage scaling
VDDC active	0.76	0.78 (Note 5)	0.88	V	Digital supply voltage in active mode; used as upper limit for adaptive voltage scaling
VDDM retention	0.50	0.58 (Note 5)	–	V	Memories supply voltage, when memories are in retention mode
VDDM standby	0.76	0.80 (Note 5)	–	V	Memory supply voltage in standby mode
VDDM active	0.76	0.78 (Note 5)	0.88	V	Memory supply voltage in active mode (Note 6)

2. With VBAT below 1.0V, the performance will be degraded. E.g. reduced PSRR, line & load regulations.
3. At system boot, VBATOD is internally connected to VBAT for 5 ms. In case VBATOD is supplied at 1.8 V and VBAT is supplied at 1.25 V, a current of ~130 mA will flow from VBATOD to VBAT. This current does not represent a reliability risk for a typical usage of the chip of 10 boots per day over 10 years.
4. With VDDO below 1.0 V, the performance will be degraded, e.g. the drive strength will be reduced.
5. These values indicate the target trimming values.
6. The VDDM voltage should be higher or equal to the core voltage (VDDC).

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = 1.25 V. The system clock (SYS_CLK) was set to 15.36 MHz. Parameters marked as screened are tested on each chip.

CURRENT CONSUMPTION

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Current consumption	I_{VBAT}	CFX load 97%, Arm Cortex−M3 processor load 40%, HEAR load 77%, Filter Engine load 9% 2 ADC @ 20 kHz, 1 OD, 1 LSAD SYS_CLK=15.36 MHz, CCO mult = 2	−	0.7	0.9	mA	✔
Standby Current	I_{STDB}	Using **onsemi**'s macro	−	90	120	μA	✔
CFX power consumption	I_{CFX}	Running 31−tap FIR, processing 4 output points in parallel	−	13.7	−	μA/MHz	
Arm Cortex−M3 processor power consumption	I_{CM3}	Running 31−tap FIR, taking advantage of symmetrical coefficients	−	8.3	−	μA/MHz	
HEAR power consumption	I_{HEAR}	Running 31−tap FIR, HEAR FIR_R function	−	18.7	−	μA/MHz	
Filter Engine power consumption	I_{FENG}	Running 31−tap FIR	−	12.0	−	μA/MHz	
LPDSP32 power consumption	$I_{LPDSP32}$	Running G.722 decoding	−	10.0	−	μA/MHz	
NNA power consumption	I_{NNA1}	256−input, 256−output layer, tanh activation function, 8−bit inputs and outputs, 8−bit uncompressed weights	−	17.5	−	μA/MHz	
	I_{NNA2}	256−input, 256−output layer, tanh activation function, 8−bit inputs and outputs, 4−bit logarithmic encoded weights	−	19.7	−	μA/MHz	

NOTE: SYS_CLK = 15.36 MHz using adaptive voltage scaling.

NOTE: Currents are on VBAT at 1.25 V

VREG

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Output voltage	VREG	50 μA < I_{LOAD} < 200 μA, trimmed bandgap (Note 7)	0.89	0.9	0.91	V	✔
Load current	I_{LOAD}		−	−	2	mA	
Line regulation	$LINE_{REG}$	I_{LOAD} = 1 mA	−	−	5	mV/V	
Load regulation	$LOAD_{REG}$	5 μA < I_{LOAD} < 2 mA	−	6	10	mV/mA	
PSRR @ 1 kHz	PSRR	I_{LOAD} = 1 mA, VBAT > 1.05 V	80	−	−	dB	

7. VBAT ≥ 1 V is required to have VREG at 0.9 V. Trimming steps: 5 mV. The typical (Typ) value shown for VREG is its target trimming value.

VDDA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Output voltage	VDDA	Standby Mode (STBY), I_{LOAD} < 100 μA, VBAT > 0.90 V	1.7	1.8	1.9	V	✔
		Low−Power Mode (LPM), I_{LOAD} = 100 μA, VBAT > 0.92 V	1.7	1.8	1.9	V	
		High-Power Mode (HPM), I_{LOAD} < 4 mA, VBAT > 0.95 V	1.7	1.8	1.9	V	✔
Typical output voltage trimming range	$VDDA_{RANGE}$	LPM, Typical Process, 25°C, VBAT = 1.25 V; I_{LOAD} = 100 μA	1.57	–	1.98	V	
Trimming steps	$VDDA_{STEP}$		–	6.5	–	mV	
Load current	I_{LOAD}	STBY	–	–	100	μA	
		LPM	–	100	500	μA	
		HPM	–	–	4	mA	
Load regulation	$LOAD_{REG}$	LPM, VBAT = 1.20 V; 100 μA < I_{LOAD} < 500 μA	–	4	10	mV/mA	
		HPM, VBAT = 1.20 V; 1 mA < I_{LOAD} < 2 mA	–	4	10	mV/mA	
Line regulation	$LINE_{REG}$	SDBY, 1.2 V < VBAT < 1.86 V; I_{LOAD} = 100 μA	–	10	36	mV/V	
		LPM, 1.2 V < VBAT < 1.86 V; I_{LOAD} = 100 μA	–	4	10	mV/V	
		HPM, 1.2 V < VBAT < 1.86 V; I_{LOAD} = 1 mA	–	4	10	mV/V	
PSRR	$VDDA_{PSSR}$	VBAT = 1.2 V; @ 1 kHz	40	–	–	dB	

VDDIF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Output voltage (high−power mode)	VDDIF	VBAT > 0.95 V; I_{LOAD} < 5 mA (Note 8)	1.7	1.8	(2xVBAT − 100 mV) (Note 9)	V	
		VBAT > 1.05V; I_{LOAD} < 15 mA	1.7	1.8	(2xVBAT − 200 mV) (Note 9)	V	✔
Typical output voltage trimming range	$VDDIF_{RANGE}$		1.57	–	1.98	V	
Trimming steps	$VDDIF_{STEP}$		–	6.5	–	mV	
Load current	I_{LOAD}	Low−power mode	–	–	1	mA	
		High−power mode	–	–	15	mA	
Load regulation	$LOAD_{REG}$	VBAT = 1.2 V; HPM, I_{LOAD} = 5 mA	–	5	10	mV/mA	
		VBAT = 1.2 V; LPM; I_{LOAD} = 500 μA	–	17	20	mV/mA	
Line regulation	$LINE_{REG}$	VBAT > 1.2 V; I_{LOAD} = 100 μA	–	4	20	mV/V	
PSRR	$VDDIF_{PSSR}$	VBAT = 1.2 V; @ 1 kHz, I_{LOAD} = 5 mA	30	–	–	dB	

8. VBAT voltage on IC pin
9. VDDIF max can't exceed 1.98 V

NOTE: Low Power Mode (LPM): Switching frequency = 128 kHz / itrim = 0X00
High Power Mode (HPM): Switching frequency = 320 kHz / itrim = 0X10

VMIC

The output voltage on the VMIC pin can be chosen from 5 different sources:

- VMIC regulator powered by VBAT
- VMIC regulator powered by VDDA
- VREG
- VDDA
- VDDIF

VMIC

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Switch impedance	$VMIC_{IMP}$	Measured with a 250 μA load current	50	100	250	Ω	
Typical output voltage trimming range	VMIC	Regulator powered by VBAT. Maximum Output: VBAT−0.1 V	0.8	–	1.3	V	✔
		Regulator powered by VDDA	0.8	–	1.3	V	✔
Trimming steps	$VMIC_{STEP}$		–	25	–	mV	
Load current	I_{LOAD}		–	–	500	uA	
Line regulation	$LINE_{REG}$		–	–	10	mV/V	
Load regulation	$LOAD_{REG}$		–	5	10	mV/mA	
Regulator VDDA PSRR	$VMIC_{PSSR}$	Regulated from VDDA	60	–	–	dB	
Regulator VBAT PSRR		Regulated from VBAT, VBAT−VMIC > 0.1 V	80	–	–	dB	

NOTE: The resistor between GND_MIC and VSSA is 50 Ohm.

VDDOD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Typical output voltage trimming range	VDDOD	Maximum Output: VBAT−0.2 V	0.8	–	1.4	V	✔
Trimming steps	$VDDOD_{STEP}$		–	25	–	mV	
Load current	I_{LOAD}		–	–	25	mA	
Line regulation	$LINE_{REG}$		–	–	10	mV/V	
Load regulation	$LOAD_{REG}$		–	1	10	mV/mA	
PSRR	$VMIC_{PSSR}$		40	–	–	dB	

NOTE: We recommend to always enable the VDDOD regulator. It improves the PSRR when large transient currents are drawn elsewhere in the Ezairo 8300 based system and gives an audio output level that is independent of the battery voltage.

VDDM/VDDC

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Typical output voltage trimming range	$VDDM_{RANGE}$, $VDDC_{RANGE}$	(Note 10)	0.45	–	0.88	V	✔
Trimming steps	$VDDM_{STEP}$, $VDDC_{STEP}$		–	2	–	mV	
Load regulation	$LOAD_{REG}$		–	7	10	mV/mA	
Line regulation	$LINE_{REG}$		–	–	10	mV/V	
Load current	I_{LOAD}		–	–	5	mA	
PSRR @ 1 kHz	$VDDM_{PSRR}$, $VDDC_{PSRR}$	VBAT = 1.25 V, VDDC/M = 0.80 V, I_{LOAD} = 500 μA	25	–	–	dB	

10. The voltage of VDDC and VDDM shall not go beyond the values specified in the operating conditions.

REGULATORS TEMPERATURE STABILITY

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Temperature Stability		Temperature range of −5 to 50°C.	−0.5	–	0.5	%	

NOTE: Temperature stability for VREG, VDDA (LPM and HPM), VMIC, VDDOD, VDDC (using the band gap as reference) and VDDM (using the band gap as reference):

REGULATORS TEMPERATURE STABILITY

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Temperature Stability		Temperature range of −5 to 50°C.	−2	–	2	%	

NOTE: Temperature stability for VDDA (STBY), VDDC (using the PMU as reference) and VDDM (using the PMU as reference):

POWER−ON−RESET

Description	Symbol	Conditions	Min	Typ	Max	Unit	Screened
VBAT startup voltage: High threshold voltage	Vth_{High}		0.68	0.77	0.86	V	✔
VBAT shutdown voltage: Low threshold voltage	Vth_{Low}		0.63	0.72	0.81	V	✔

NOTE: Typical time duration between application of VBAT and first NVM access: 77 ms

INPUT STAGE

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Nominal input referred noise 16 kHz SF, RMS	IN_{IRN}	A−weighted 100 Hz−8 kHz, 16 kHz SF, nominal current setting	–	2	4	μVrms	
Nominal input referred noise 32 kHz SF, RMS		A−weighted 100 Hz−16 kHz, 32 kHz SF, maximum current setting	–	3	10 (Note 11)	μVrms	✔
HiQ input referred noise 16 kHz SF, RMS		A−weighted 100 Hz−8 kHz, 16 kHz SF, maximum current setting	–	1.5	3	μVrms	
HiQ input referred noise 48 kHz SF, RMS		A−weighted 20 Hz−20 kHz, 48 kHz SF, maximum current setting	–	3	10 (Note 12)	μVrms	✔
Nominal dynamic range	IN_{DR}	A−weighted 100 Hz−8 kHz, nominal current setting	–	109	–	dB	
HiQ dynamic range		A−weighted 100 Hz−8 kHz, maximum current setting	–	112	–	dB	
Input range	IN_{RANGE}	At VDDA 1.8 V	0	–	1.6	V	
Input impedance	R_{IN}	Nominal and HiQ mode	10	–	–	MΩ	
Peak THDN	IN_{THDN}		–	−85	−70	dB	✔
Channel gain mismatch		Calibrated (using digital gain factor, 1 kHz) or not calibrated.	–	–	0.1	dB	
Channel delay mismatch		At 1 kHz (approx. max 0.54 deg)	–	–	1.5	μs	
Ultrasonic immunity, input referred aliased level		A−weighted 100 Hz − 16 kHz aliased level with a −40 dBV input signal swept from 20 kHz to 50 kHz	–	−95	−85	dBV	
Signal detection mode input referred noise		A−weighted 100 Hz−10 kHz, 1 MHz operation, current setting at 0x1 (4 μA)	–	10	20	μVrms	
Microphone bias voltage	MIC_{BIAS}	In order to maximize dynamic range of the input stage, the microphone bias should be set to the typical value.	0.2	0.75	1.0	V	

NOTE: Input Stage specifications are A−weighted, bandwidth 100 Hz−fs/2, sampling frequencies 16/32/48 kHz, with ADC_CLK = 3.84 MHz. The CCO multiplier doesn't affect the specifications of the ADC as long as the ADC_CLK is around 4 MHz.

NOTE: The specifications at 20 kHz are between the specifications at 16 and 32 kHz.

11. By characterization, the Max value is 5 μVrms.
12. By characterization, the Max value is 5 μVrms.

OUTPUT STAGE

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Output resistance	R_{OD}	I_{LOAD} = 1 mA. High and Low side combined.	–	2	–	Ω	
Output Dynamic Range	OD_{DR}	High impedance load (>1 kΩ), XSDM0 mode	103	108	–	dB	
		Low impedance speaker mode, 36R load, XSDM0 mode	–	105	–	dB	
		High impedance load (>1 kΩ), OD_DELAY mode	95	100	–	dB	
Peak THD+N	OD_{THDN}	@ 1 kHz, high impedance load (>1 kΩ), XSDM0 mode	–	−72	−61 (Note 13)	dB	✔
		@ 1 kHz, low impedance speaker mode, 36R load, XSDM0 mode	–	−61	–	dB	
		@ 1 kHz, high impedance load (>1 kΩ), OD_DELAY mode	–	−81	−75	dB	
Output noise RMS	OD_{ORN}	At 1.25 V VBATOD; scales linearly with VBATOD	–	–	4.3	μV	
Output Bandwidth	OD_{BW}		–	–	24	kHz	
Maximum output current	I_{OD}	This current can be drawn but with degraded audio quality.	–	–	25	mA	
Power supply rejection ratio (PSRR)	OD_{PSRR}		–	−30	–	dB	
		Using VDDOD regulator	–	−85	−75	dB	

NOTE: Output stage specifications are A−weighted, bandwidth 100 Hz−fs/2, sampling frequencies 16/32/48 kHz, with SDM_CLK = 15.36 MHz, SYS_CLK = 15.36 MHz (CCO multiplier = 1), and with VDDOD = 1.0 V

NOTE: The performances of the OD are optimized when the SDM_CLK operates on the CCO base frequency (the un−multiplied frequency).

13. By characterization, the Max value is −65 dB.

LSAD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
ADC Resolution	$LSAD_{RES}$	Depends on frequency setting	8	12	14	Bits	
Input signal level	$LSAD_{RANGE}$		0	–	1.8	V	✔
Sampling rate	$LSAD_{SF}$	For a sample clock of 128 kHz (20 cycles per measurement)	–	6.4	–	kHz	
lsad_clk frequency	$LSAD_{CLK}$		–	100	128	kHz	
INL	$LSAD_{INL}$		−2	–	+2	mV	
DNL	$LSAD_{DNL}$		−1	–	+1	mV	
Input Impedance	$LSAD_{INI}$		1	–	–	MΩ	

IOs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Voltage level of high input	V_{IH}		–	–	0.7x VDDO	V	✔
Voltage level of low input	V_{IL}		0.3x VDDO	–	–	V	✔
Voltage level of high output	V_{OH}		0.8x VDDO	–	VDDO	V	✔
Voltage level of low output	V_{OL}		VSSO		0.2x VDDO	V	✔
Weak pull−up Impedance	IMP_{WUP}		225	250	275	kΩ	✔
Medium pull−up Impedance	IMP_{MUP}		45	50	60	kΩ	✔
Medium pull−down Impedance	IMP_{MDW}		45	50	60	kΩ	✔

IOs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Strong pull−up Impedance	IMP_{SUP}		0.8	1	1.2	kΩ	✔
Pad Input Delay	IN_{DELAY}	VDDO=1.8V	−	−	0.76	ns	
		VDDO=1.2V	−	−	1.23	ns	
Pad Output Delay	OUT_{DELAY}	VDDO=1.8V 1x drive strength, 1 pF load 2x drive strength, 2 pF load 4x drive strength, 4 pF load 8x drive strength, 8 pF load	−	−	1.24	ns	
		VDDO=1.2V 1x drive strength, 1pF load 2x drive strength, 2 pF load 4x drive strength, 4 pF load 8x drive strength, 8 pF load	−	−	1.74	ns	
Drive Strength	DRIVE	Configurable with 1x, 2x, 4x, 8x Nominal drive strength: 1 mA	1	−	8	Multiple of the nominal drive strength	
Max Switching Frequency	$IOFR_{Max}$		Maximum SYS_CLK	−	−		
Glitch filter : additional rise delay	$DELAY_{RAISE}$		−	−	169	ns	
Glitch filter : additional fall delay	$DELAY_{FALL}$		−	−	245	ns	

NOTE: DC Characteristics of the digital pad at VDDO 1.08/1.8/1.98V

NOTE: The glitch filter cuts glitches with duration shorter than 50 ns

CURRENT CONTROLLED OSCILLATOR (CCO)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Recommended Working Frequency	SYS_CLK	For recommended VDDC and VDDM	2.56	−	61.44	MHz	
Boot frequency	SYS_CLK		5	7.68	10	MHz	✔
Oscillator frequency trimming precision			−	0.10	0.20	%	
Frequency stability in temperature		Temp: 0°C and 50°C. After calibration at room temperature (25°C)	−1.5	−	1.5	%	
		Temp: −40°C and 85°C. After calibration at room temperature (25°C)	−4	−	4	%	
Period jitter (rms)		RMS, at 5.12 MHz, before multiplication	−	−	200	ps	
		RMS, at 5.12 MHz, after multiplied by 2 and divided by a multiple of 2	−	−	200	ps	
		RMS, at 5.12 MHz, after multiplied by 4 and divided by a multiple of 4	−	−	200	ps	
Output duty cycle		With multiplier setting 1x or 2x	45	−	55	%	
		With multiplier setting 4x	40	−	60	%	
Max frequency		Un−multiplied	−	30	−	MHz	

LOW DELAY PATH (using the low delay path of the Filter Engine)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Screened
Analog to analog delay		Fs=48kHz FENG delay: one sample	−	10.4	−	μs	

EZAIRO 8300 INTERNAL ARCHITECTURE

The architecture of the Ezairo 8300 is shown on the following diagram:

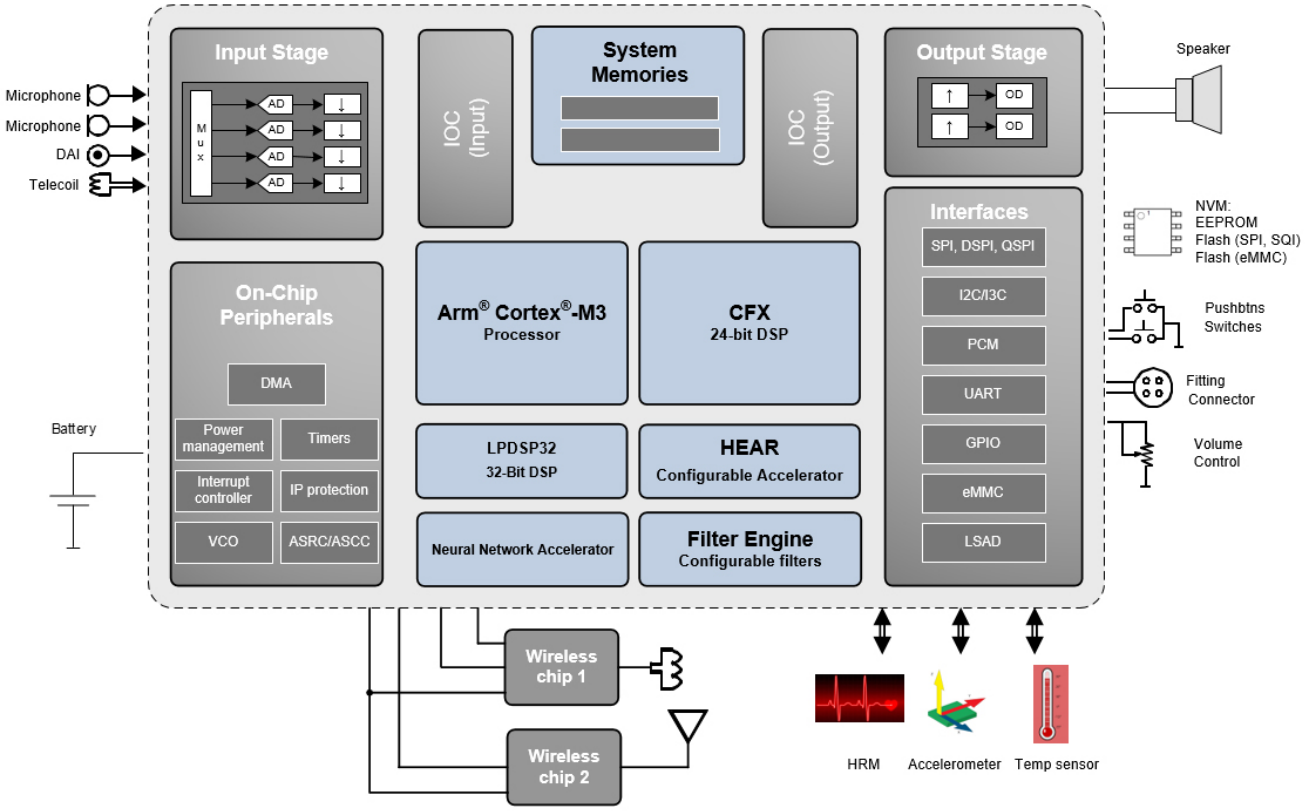


Figure 1. Ezairo 8300 Architecture

ARCHITECTURE OVERVIEW

The Ezairo 8300 system is an asymmetric 6−core architecture, mixed−signal system−on−chip designed specifically for the audio processing needs ultra−lower power portable devices. It centers around 6 processing cores: the CFX Digital Signal Processor (DSP), the Arm Cortex−M3 Processor, the LPDSP32 Digital Signal Processor (DSP), the HEAR Configurable Accelerator, the Filter Engine and the Neural Network Accelerator.

CFX DSP Core

The CFX DSP is a user−programmable general−purpose DSP core that uses a 24−bit fixed−point, dual−MAC, dual−Harvard architecture. It is able to perform two MACs, two memory operations and two pointer updates per cycle, making it well−suited to computationally intensive algorithms.

The CFX DSP is used for custom signal processing applications. The CFX DSP core can also be used as the master of the Ezairo 8300 SoC, by configuring the system and the other cores, by managing the Interrupts and by coordinating the flow of signal data progressing through the system.

The CFX features:

- Dual−MAC 24−bit load−store DSP core
- Four 56−bit accumulators
- Four 24−bit input registers
- Support for hardware loops nested up to four deep
- Combined XY memory space (48 bits wide)
- Dual address generator units
- A wide range of addressing modes:
  - Direct
  - Indirect with post−modification
  - Modulo addressing
  - Bit reverse

Software development on the CFX is done in C or assembly, and the development tools are available in the Ezairo 8300 SDK.

In cases where the Arm Cortex−M3 processor is used as the master of the system, the CFX is slave to the Arm Cortex−M3 processor. The inter−processor communication methods between the CFX processor and the rest of Ezairo 8300 are based on shared memories and interrupts.

CFX DSP Architecture

The CFX employs a parallel instruction set for simultaneous control of multiple computation units. The DSP can execute up to four computation operations in parallel with two data transfers (including rounding and/or saturation as well as complex address updates), while simultaneously changing control flow.

The CFX architecture encompasses various memory types and sizes, peripherals, interrupt controllers, and interfaces.

Figure 2 illustrates the basic architecture of the CFX. The control lines shown exiting the PCU indicate that control signals go from the PCU to essentially all other parts of the CFX.

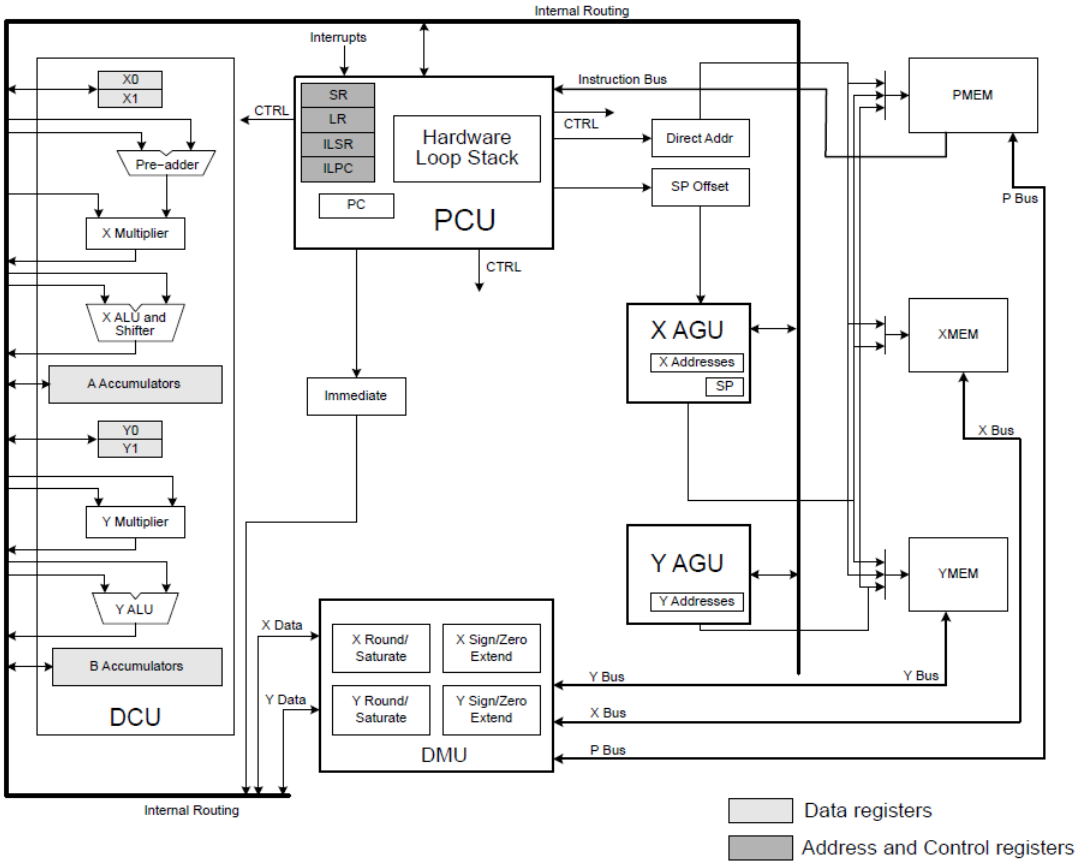


Figure 2. CFX DSP Core Architecture

Arm Cortex−M3 Processor

The Arm Cortex−M3 processor is a low−power processor that features low gate count, low interrupt latency, and low−cost debugging. It is intended for deeply embedded applications that require fast interrupt response features.

GNU tools provide build and link support for C programs that run on the Arm Cortex−M3 processor.

The Arm Cortex−M3 processor implements the ARMv7−M architecture. For power management, the processor can be placed into a sleep mode under firmware control in which the processor clock is disabled. The Nested Vectored Interrupt Controller (NVIC) continues to run to enable exiting sleep on an interrupt.

The Arm Cortex−M3 processor typically performs one or more of the following roles:

- The system master, configuring the system and the other cores, by managing the interrupts, and by coordinating the flow of signal data progressing through the system
- A coprocessor to the CFX DSP that provides additional microcontroller computation for interface drivers and protocols executing on those interfaces
- A controller for managing hardware acceleration peripherals such as the Reed−Solomon, G.722 blocks, the asynchronous sample rate converter (ASRC), the audio sink clock counters (ASCC), the neural network accelerator (NNA), or the LPDSP32 DSP (which is expected to be used for codecs, a neural network, and similar use cases).

In cases where the CFX is used as the master of the system, the Arm Cortex−M3 processor is slave to the CFX. The inter−processor communication methods between the Arm Cortex−M3 processor and the rest of Ezairo 8300 are based on shared memories and interrupts.

HEAR Configurable Accelerator

The HEAR coprocessor is designed to perform both common signal processing operations and complex standard filterbanks such as the WOLA filterbank, reducing the load on the system programmable DSP cores.

The HEAR Configurable Accelerator is a highly optimized signal processing engine that is configured through the CFX or Arm Cortex−M3 processor. It offers high speed, high flexibility and high performance, while maintaining low power consumption. For added computing precision, the HEAR supports block floating point processing. Configuration of the HEAR is performed using the HEAR Configuration Tool (HCT). For further information on the usage of the HEAR, refer to the *HEAR Configurable Accelerator Reference Manual*.

The HEAR is optimized for advanced algorithms including but not limited to the following:

- Dynamic range compression
- Directional processing
- Feedback cancellation
- Noise reduction

To execute these and other algorithms efficiently, the HEAR excels at the following:

- Processing using a weighted overlap add (WOLA) filterbank
- Time domain filtering
- Subband filtering
- Attack/release filtering
- Vector addition/subtraction/multiplication
- Signal statistics (such as average, variance and correlation)

Filter Engine

The Filter Engine is a core that provides low−delay path and basic filtering capabilities for the Ezairo 8300 system.

The Filter Engine can implement filters (either FIR or IIR) with a total of up to 320 coefficients. FIR filters are implemented using a direct−form structure. IIR filters are implemented with a cascade of second−order sections (biquads), each implemented as a direct−form I filter.

The Filter Engine is programmable, but does not include direct debugging access. The CFX and the Arm Cortex−M3 Processor can monitor the Filter Engine state through control and configuration registers on the program memory bus.

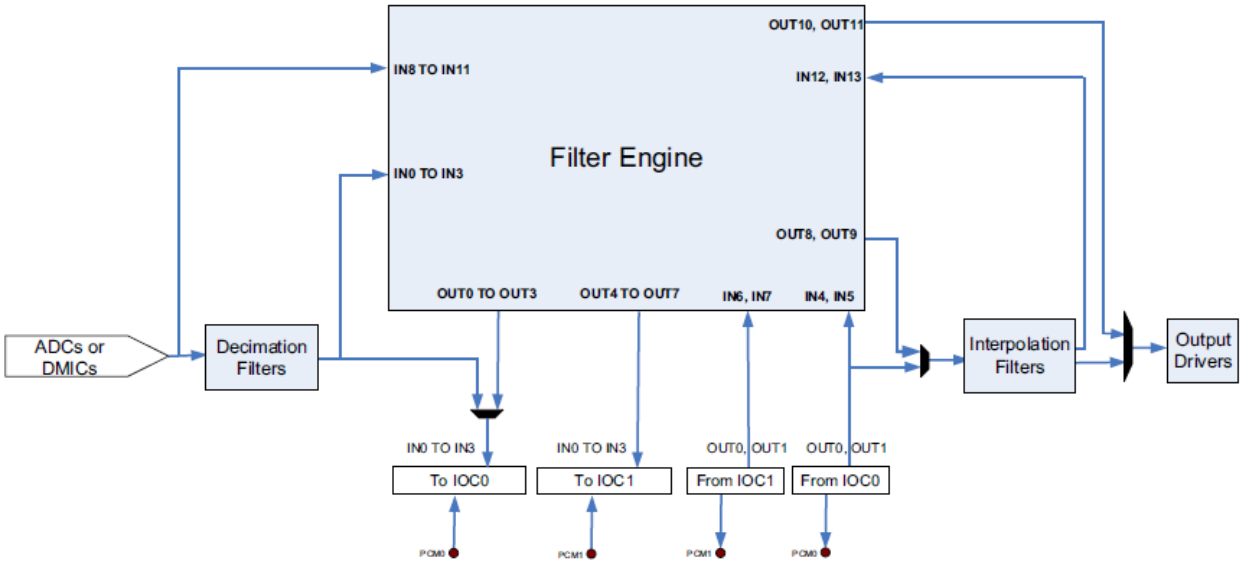


Figure 3. Filter Engine: Audio Filtering and Multipliexing

LPDSP32 DSP

LPDSP32 is a C−programmable, 32−bit DSP developed by **onsemi**. LPDSP32 is a high efficiency, dual Harvard DSP that supports both single (32−bit) and double precision (64−bit) arithmetic.

LPDSP32's dual MAC unit, load store architecture is specifically optimized to support audio processing tasks such as audio codecs that might be required for wireless audio communication tasks, Artificial Intelligence (AI) functions, and other advanced developments requiring the additional processing power that this core provides. The advanced architecture also provides:

- Two 72−bit ALUs capable of doing single and double precision arithmetic and logical operations
- Two 32−bit integer/fractional multipliers
- Four 64−bit accumulators with 8−bit overflow (extension bits)

The LPDSP32 relies on the CFX DSP or the Arm Cortex−M3 processor to initialize its memories and peripherals. Once initialized, the CFX DSP and/or the Arm Cortex−M3 processor control the LPDSP32 DSP's execution state.

Software development on the LPDSP32 is done in C.

Neural Network Accelerator (NNA)

The Neural Network Accelerator (NNA) is a hardware accelerator block that allows complex neural networks to run in an energy efficient manner. The accelerator can execute a single layer of a fully populated or sparsely populated neural network in a single task without any processor intervention. Layers with up to 1023 inputs and 1023 outputs are supported.

The NNA contains 16 multipliers, 16 accumulators, 16 input registers and 16 coefficient registers. It includes input and coefficient "fetchers" that, once configured, manage the data and coefficients memory access automatically. Support for coefficient compression/decompression and pruning is included and help minimize the amount of coefficient needed.

Memory Structure

The following figure shows the system memory structure. The individual blocks are described in the sections that follow.

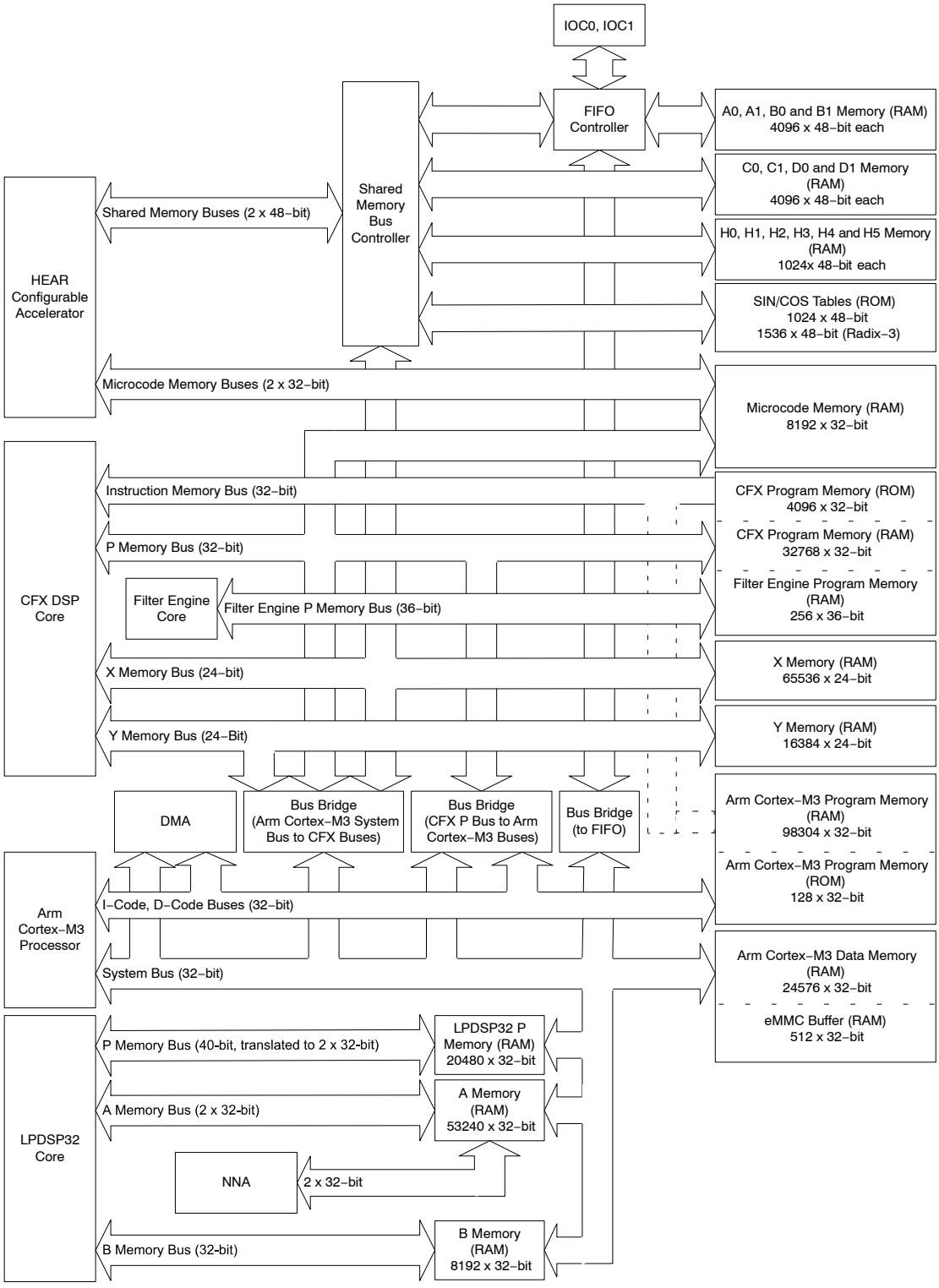


Figure 4. System Memory Architecture

FIFO Controller

The Ezairo 8300 system's FIFO controller provides the ability to define up to 32 FIFO buffers. These FIFOs are defined as up to eight FIFOs in each of the A0, A1, B0 and B1 memories.

These FIFOs may be used as:

- Input FIFOs as used by the IOC
- Output FIFOs as used by the IOC
- Intermediate FIFOs for transferring data between the CFX, HEAR and Arm Cortex−M3 processor
- Software FIFOs for the CFX DSP or Arm Cortex−M3 processor through the use of access registers
- Each individual FIFO is associated with a set of FIFO configuration registers that are mapped into X memory. Each FIFO can also be associated with one or more of the eight FIFO interrupts that are available for the CFX DSP, eight FIFO events that are available for the HEAR, and eight FIFO interrupts that are available for the Arm Cortex−M3 core.

Ezairo 8300 Memory Structure

- The following tables list the memory structures attached to the CFX, the Arm Cortex−M3 Core, the HEAR, the LPDSP32, the FENG and the eMMC interface. They include the size and width of each memory structure.

Table 4. CFX MEMORY INSTANCES

Memory Structure	Data Width	Memory Instances	Memory Size
Program memory (ROM)	32	–	4096
Program memory (RAM)	32	PRAM0, PRAM1	2 x 16384 (4 x 16384) (Note 14)
X memory (ROM)	24	–	1280
X memory (RAM)	24	–	4 x 16384
Y memory (RAM)	24	YRAM0	8192
		YRAM1, YRAM2	2 x 4096

14. The CFX program memory can be extended by assigning the Arm Cortex−M3 processor's program memory sections 0 and 1 to the CFX.

Table 5. Arm CORTEX−M3 CORE MEMORY STRUCTURES

Memory Structure	Data Width	Name	Memory Size
Program memory (ROM)	32	–	128
Program memory (RAM)	32	CM3_PRAM0 to CM3_PRAM4	5 x 16384 (3 x 16384) (Note 15)
		CM3_PRAM5, CM3_PRAM6	2 x 8192
Data memory (RAM)	32	CM3_DRAM0, CM3_DRAM1	2 x 8192
		CM3_DRAM2, CM3_DRAM3	2 x 4096

15. Sections 0 and 1 of the Arm Cortex−M3 processor's program memory can be assigned to the CFX DSP.

Table 6. HEAR Memory Structures

Memory Structure	Data Width	Name	Memory Size
Microcode memory (RAM)	32	HEAR_MICROCODE_PMEM0, HEAR_MICROCODE_PMEM1	2 x 4096
Data memory (RAM)	48	H0, H1, H2, H3, H4, H5 memories	6 x 1024
FiFo Memory (RAM)	48	A0, A1, B0, B1 memories	4 x 4096
Coefficient Memory (RAM)	48	C0, C1, D0, D1 memories	4 x 4096
Data ROM	48	SIN/COS LUT	1024
		SIN/COS Radix−3 LUT	1536

Table 7. LPDSP32 CORE MEMORY STRUCTURES

Memory Structure	Data Width	Name	Memory Size
Program memory (RAM)	32	DSP_PRAM0, DSP_PRAM1	2 x 2048
		DSP_PRAM2 to DSP_PRAM5	4 x 4096
A memory (RAM)	32	DSP_ARAM0, DSP_ARAM1	2 x 8192
		DSP_ARAM2, DSP_ARAM3	2 x 16384
		DSP_ARAM4, DSP_ARAM5	2 x 2048
B Memory (RAM)	32	DSP_BRAM0, DSP_BRAM1	2 x 2048
		DSP_BRAM2	2 x 2048

Table 8. OTHER MEMORY STRUCTURES

Memory Structure	Data Width	Memory Size
FENG Program memory (RAM)	36	256
eMMC interface buffer (RAM)	32	512
Filter Engine State	24	320
Filter Engine Temp	28	64
Filter Engine Coefficients	28	320

Input/Output Controllers (IOC)

The IOCs are responsible for handling input/output audio data. Samples can be routed along a number of different paths using the multiplexing options available in the Ezairo 8300 system.

Direct Memory Access (DMA) Controller

The direct memory access controller (DMA) module allows background data transfers between components on the peripheral bus and memories without any processor intervention. This allows the processors to be used for other computational needs while enabling high speed sustained transfers to and from the peripherals/memories. The DMA has 8 independent configurable channels.

Each channel can be configured for one of four modes:

- Data transferred from peripheral−to−memory
- Data transferred from memory−to−peripheral
- Data transferred between peripherals
- Data transferred between memory locations

Interrupts

The Ezairo 8300 system contains an interrupt controller linked to the CFX DSP. This controller services all of the Ezairo 8300 interrupt sources, except the private peripheral interrupts and faults of the Arm Cortex−M3 processor.

The Arm Cortex−M3 processor can be used as the master of the Ezairo 8300 system. The Arm Cortex−M3 processor is closely tied to a nested vectored interrupt controller (NVIC), which is an integral part of the processor and provides the interrupt handling functionality. The NVIC services the private peripheral interrupts and faults of the Arm Cortex−M3 processor and all other Ezairo 8300 interrupt sources. The LPDSP32 is linked to an interrupt controller that services interrupts from the DMA, inter−processor communications, and the NNA.

Hear Function Chain Controller

The HEAR function chain controller responds to commands from the CFX or from the Arm Cortex−M3 processor, and events from the FIFO controller. It must be configured by the CFX or by the Arm Cortex−M3 processor to enable the triggering of particular function chains within a microcode configuration.

Timers

The Ezairo 8300 system provides five timers, including:

- The SysTick timer from the Arm Cortex−M3 processor
- Four general−purpose timers, each of them providing:
  - A 24−bit counter
  - A 3−bit prescale factor that increases by a factor of 2 at each step, scaling between a prescaler of 1 and 128.
  - Three operating modes: single−shot/multiple−shot, free−run, and DIO interrupt capture
  - A dedicated interrupt that can be used to signal timer expiration
  - Dedicated configuration and status registers

Watchdog Timer

The watchdog timer is a programmable hardware timer that operates from the system clock and is used to ensure system sanity. It is always active and must be periodically acknowledged as a check that an application is still running.

Once the watchdog times out, it generates an interrupt. If left to time out a second consecutive time without acknowledgement, a system reset will occur.

Algorithm and Data Security

Algorithm software code and user data that requires permanent retention is stored off the Ezairo 8300 chip in separate non−volatile memory. To support this, the Ezairo 8300 chip can gluelessly interface to an external SPI, DSPI or QSPI EEPROM, Flash, or eMMC flash (referred here as external non−volatile memory or NVM).

To prevent unauthorized access to the sensitive intellectual property (IP) stored in the external non−volatile memory, a comprehensive system is in place to protect manufacturer's application code and data.

To protect the IP stored in the external non−volatile memory, the system supports decoding algorithm and data sections belonging to an application that have been encrypted using the Advanced Encryption Standard (AES) and stored in non−volatile memory. While system access restrictions are in place, the keys used in the decryption of these sections will be secured from external access by the regular access restrictions.

When the system is externally "unlocked" these keys will be cleared, preventing their use in decoding an application by unauthorized parties. After un−restricting access in this way the system may then be restored by re−programming the decryption keys.

Input Stage

The input stage of an Ezairo 8300 provides four audio input channels that supply signal data to the rest of the Ezairo 8300 system. Each input channel includes:

- Input selection using an analog multiplexer to select between the input source from the available input sources and reference inputs
- Available line−out for the selected input signal
- An over−sampling analog−to−digital converter (ADC) which uses a programmable sampling frequency and provides a configurable sampling delay, useful in beam−forming applications.
- Selectable digital microphone inputs and bypass registers that can source data in place of the ADCs
- High−quality decimation filtering at all selectable sampling rates
- Selectable input muting

Each of the input channels from the Ezairo 8300 system can optionally source their input data from a digital microphone (DMIC input) instead of the channel's ADC.

Output Stage

The output stage of Ezairo 8300 provides two audio output channels that post−process signal data from the rest of the Ezairo 8300 system, and provide it to external receivers or speakers. The output channels include:

- High−quality interpolation filtering that automatically tracks the selected sample rate of the sigma−delta Modulator
- An ultra−low−power, high fidelity, over−sampled sigma−delta modulator with programmable sample rate
- A low−impedance direct digital output driver, driven by a pulse−density modulated signal, for zero−bias hearing aid or headset receivers
- Selectable digital microphone outputs that can sink data in parallel with either output channel

Digital Input/Output (DIO) Pads

The Ezairo 8300 system contains 36 digital input/output (DIO) pads that can be configured:

- To support the external interfaces, output clocks, and other I/Os
- As general−purpose I/Os (GPIO)
- Analog input/output function

The 36 DIOs are split into four power domains. The voltages for these 4 power domains are given by the VDDO1 pad (for DIO0 to DIO11), the VDDO2 pad (for DIO12 to DIO23), the VDDO3 pad (for DIO24 to DIO29) and the VDDO4 pad (for DIO30 to DIO35).

The NRESET, SDA and SCL pads are on the VDDO4 power domain.

EXTERNAL INTERFACEs

General−Purpose Input/Output (GPIO)

Ezairo 8300 can configure any, or all, of the 36 DIO pads as software−controlled general−purpose DIO (GPIO) pads. The function of these GPIO pads is defined by the user application, which can use them for any general−purpose input or output. Each GPIO pad can be configured to generate interrupts to the CFX DSP and/or Arm Cortex−M3 processor.

PCM Interface

The Ezairo 8300 system includes two highly−configurable pulse code modulation (PCM) interfaces that can be used to stream signal, control and configuration data in and out of the device.

Each PCM interface connects to the processors through the Arm Cortex−M3 processor's peripheral bus. There are three possible ways PCM interfaces can handle transmission and reception buffers:

- By using the internally available data transmission and reception interrupts.
- By connecting to the DMA with two channels supporting transmit and receive operations.
- By connecting to the IOC with four FIFOs supporting transmit and receive operations. Each data channel for PCM transmit and receive buffers requires its own FIFO−as opposed to the case for using DMA, which allows one DMA channel to support both channel 0 and channel 1 for PCM.

Each PCM interface can be configured to generate interrupts to the CFX DSP and/or Arm Cortex−M3 processor.

SPI Interface

The Ezairo 8300 system includes two Serial Peripheral Interfaces (SPIs). Each SPI interface supports single and dual I/O modes, as well as the ability to add two additional I/O pins in a quad I/O mode.

The SPI interfaces allow the system to communicate with external components, including external analog front ends, external controllers, wireless transceivers, and non−volatile memories (NVMs).

The SPI interfaces support master/slave configuration as well as half/full duplex mode.

Each SPI interface can be configured to generate interrupts to the CFX DSP and/or Arm Cortex−M3 processor. Similarly, data transfers can be controlled by any of the host processors.

UART Interface

The general−purpose UART interface provides support for communicating with devices that use standard UART and RS−232 transmission protocols.

The UART Interface can be configured to generate interrupts to the CFX DSP and/or Arm Cortex−M3 processor. Similarly, data transfers can be controlled by any of the host processors.

Low−Speed A/D Converters (LSAD)

The purpose of the LSAD converters is to sample voltages that typically change slowly, such as the voltage associated with a potentiometer−based volume control.

The LSADs provide an analog to digital conversion of up to eight signals, from a combination of four internal signals

and four external signals. The LSAD provided 14 bits of resolution, at sampling rates up to 8 kHz.

The LSAD can be configured to generate interrupts to the CFX DSP and/or Arm Cortex−M3 processor. Similarly, data can be read by any of the host processors.

I²C Interface

The Ezairo 8300 includes 3 instances of I²C interface, which are compatible with the Inter−IC Bus Specification from NXP Semiconductors. I²C interfaces are typically used for communication with external sensors and storage devices, and as control signals for wireless radios.

The I²C Interface can be configured to generate interrupts to the CFX DSP and/or Arm Cortex−M3 processor. Similarly, data transfers can be controlled by any of the host processors. Maximum I²C SCL frequency is provided in the Ezairo 8300 Hardware Reference Manual.

I³C Interface

The Ezairo 8300 includes 2 instances of I³C interface which are compatible with the Improved Inter−IC Bus Specification from the MIPI Alliance. The I³C uses a two−wire interface including a bidirectional clock line (SCL) and a bidirectional data line (SDA). I³C is designed to enhance sensor system design architectures in mobile wireless products by providing a fast, low cost, low power, two−wire digital interface for sensors.

The I³C Interface can be configured to generate interrupts to the CFX DSP and/or Arm Cortex−M3 processor. Similarly, data transfers can be controlled by any of the host processors.

eMMC Interface

eMMC memory (Embedded MultiMedia Card memory) is a low−cost, high performance Flash memory that is designed for a wide range of applications in consumer electronics such as mobile phones, handheld computers, navigational systems, portable gaming and even industrial uses.

The eMMC interface of Ezairo 8300 implements the Host Controller portion of an eMMC link and can also be used to access SD cards.

The eMMC Interface can be configured to generate interrupts to the CFX DSP and/or Arm Cortex−M3 processor. Similarly, data transfers can be controlled by any of the host processors.

Debug Ports

I2C Debug Ports for the CFX and the Arm Cortex−M3

The I2C debug ports for the Ezairo 8300 system provide both the CFX DSP and Arm Cortex−M3 processor with a full debugging capacity.

The CFX DSP debug port coexists with the Arm Cortex−M3 processor debug port on the same I2C bus. One of the three general purpose I2C interface can be used on the same bus. Each debug port will respond to debug commands on its I2C address.

SWJ−DP Debug Port for the Arm Cortex−M3

The Ezairo 8300 system contains a standard Core Sight SWJ−DP debug port for the Arm Cortex−M3 processor. This debug controller is used to provide access to all of the Arm Cortex−M3 processor registers, and to all of the Ezairo 8300 memories through the memory buses attached to the Arm Cortex−M3 processor. By default, the SWJ−DP is accessed using the JTAG connection that uses DIOs 30 to 33, to form a 4−wire JTAG interface. This debug port can be reconfigured for serial−wire mode using only DIOs 30 and 31.

The Arm Cortex−M3 processor's SWJ−DP debug port can be used as a bridge to the CFX I²C debug port through a memory−mapped register.

Standard JTAG debug port for the LPDSP32

The LPDSP32 is supported by a JTAG debug interface that can be assigned to a set of DIO pads.

Other Peripherals

Clock−Generation Circuitry and Synchronization

The main system clock is typically generated by a current−controlled oscillator (CCO) that can be configured for frequencies from 1.28 MHz to 61.44 MHz. Other needed clocks are derived from the main system clock.

An Asynchronous Sample Rate Converter (ASRC) and Audio Sink Clock Counters blocks to provide a means of synchronizing the audio sample rate between the radio link and the host device.

Power Supervisory Unit

The power supervisory unit monitors the battery supply voltage (VBAT) and the internal analog and digital supply voltages (VDDA, VDDC, VDDM), safely shutting down the system without user intervention when the supply voltages are below the thresholds required for valid system operation.

This unit is used to ensure that the system operates correctly and is not damaged by the power supply fluctuations that are encountered when a battery is inserted or removed from a hearing aid.

Power−on−Reset (POR)

The Ezairo 8300 device uses a power−on−reset (POR) sequence to ensure proper system behavior during startup, and to ensure proper system configuration after startup. At the start of the POR sequence, audio output is disabled and all configuration and control registers are asynchronously reset to their default values.

At the start of the POR sequence, the core registers for all five of the system's cores are cleared and the contents of all RAM is unspecified.

EZAIRO 8300 PAD SPECIFICATIONS

Pad Name	Description	Power Domain	Type	Pull	Pad #, WLCSP	Pad #, BGA
VBAT	Battery input voltage	VBAT	P		C2, D2	D6, C7, D7
VDDA	Analog power supply	VDDA	P		B2	B8
VDDA_C0	Analog charge pump cap terminal 0		A		C1	B9
VDDA_C1	Analog charge pump cap terminal 1		A		B1	A9
VREG	Regulated voltage output		AO		A1	B7
VMIC	Microphone power supply		AO		B3	B6
VSSA	Analog ground		P		B4	A8, C6
GNDMIC	Input Transducer ground		AO		B5	B5
AI0	ADC analog input 0		AI		A2	A7
AI1	ADC analog input 1		AI		A3	A6
AI2	ADC analog input 2		AI		A4	A5
AI3	ADC analog input 3		AI		A5	A4
VDDIF	Interface power supply	VDDIF	P		E2	D8
VDDIF_C0	Interface power supply cap terminal 0		A		D1	D9
VDDIF_C1	Interface power supply cap terminal 1		A		E1	C9
OD0_P	Output Driver: Receiver Output 0 Positive	VBATOD	AO		F1	E8
OD0_N	Output Driver: Receiver Output 0 Negative		AO		G1	F8
OD1_P	Output Driver: Receiver Output 1 Positive		AO		H1	G8
OD1_N	Output Driver: Receiver Output 1 Negative		AO		J1	H8
VBATOD	Output driver power supply		P		H2, J2	F9 ,G9
VSSOD	Output driver ground		P		G2, K1	E9, H9, J9
DIO30	Digital input / output 30	VDDO4	I/O	U	J4	F6
DIO31	Digital input / output 31		I/O	U	K4	G6
DIO32	Digital input / output 32		I/O	U	L4	H6
DIO33	Digital input / output 33		I/O	U	H3	E6
DIO34	Digital input / output 34		I/O	U	J3	F7
DIO35	Digital input / output 35		I/O	U	K3	H7
VDDO4	I/O domain 4 power supply		P		L3	J6
NRESET	Reset pin		I	U	K2	G7
SDA	Debug port data		I/O	U	L2	J7
SCL	Debug port clock		I	U	L1	J8
DIO24	Digital input / output 24	VDDO3	I/O	U	K7	H3
DIO25	Digital input / output 25		I/O	U	L7	J3
DIO26	Digital input / output 26		I/O	U	J6	G3
DIO27	Digital input / output 27		I/O	U	K6	J4
DIO28	Digital input / output 28		I/O	U	J5	G5
DIO29	Digital input / output 29		I/O	U	K5	H4
VDDO3	I/O domain 3 power supply		P		L5	J5

EZAIRO 8300 PAD SPECIFICATIONS

Pad Name	Description	Power Domain	Type	Pull	Pad #, WLCSP	Pad #, BGA
DIO12	Digital input / output 12	VDDO2	I/O	U	F8	D4
DIO13	Digital input / output 13		I/O	U	G8	E2
DIO14	Digital input / output 14		I/O	U	G9	F2
DIO15	Digital input / output 15		I/O	U	H7	F4
DIO16	Digital input / output 16		I/O	U	H8	F3
DIO17	Digital input / output 17		I/O	U	H9	F1
DIO18	Digital input / output 18		I/O	U	J7	G4
DIO19	Digital input / output 19		I/O	U	J8	G2
DIO20	Digital input / output 20		I/O	U	K8	H2
DIO21	Digital input / output 21		I/O	U	K9	H1
DIO22	Digital input / output 22		I/O	U	L8	J2
DIO23	Digital input / output 23		I/O	U	L9	J1
VDDO2	I/O domain 2 power supply		P		J9	G1
VDDM	Memory power supply	NA	P		F9	E1
DIO0	Digital input / output 0	VDDO1	I/O	U	A7	B3
DIO1	Digital input / output 1		I/O	U	A8	A2
DIO2	Digital input / output 2		I/O	U	A9	A1
DIO3	Digital input / output 3		I/O	U	B7	C5
DIO4	Digital input / output 4		I/O	U	B8	B2
DIO5	Digital input / output 5		I/O	U	C7	C4
DIO6	Digital input / output 6		I/O	U	C8	C3
DIO7	Digital input / output 7		I/O	U	C9	C2
DIO8	Digital input / output 8		I/O	U	D7	D5
DIO9	Digital input / output 9		I/O	U	D8	D3
DIO10	Digital input / output 10		I/O	U	D9	C1
DIO11	Digital input / output 11		I/O	U	E8	D2
VDDO1	I/O domain 1 power supply		P		B9	B1
RESERVED	RESERVED		I	D	B6	B4
VDDC	Digital core power supply	NA	P		E9	D1
VSSO	IO Ground		P		A6, G6, F7, L6	A3, C8, E3, E7, H5
VSSC	Digital Core Ground		P		E5, F2, F3, F4	

NOTES: Legend:
Type: A=analog; D=digital; I=input; O=output; P=power
Active: H=active high; L=active low
Pull: U=pull up; D=pull down
All digital pads have a Schmitt trigger input
SCL, SDA and all DIO pads have a programmable I2C low pass filter
VSSO is the ground of all four IO power domains
Center WLCSP ground bumps (E5, F3, F4, F7, G6) are optional to be connected
Dummy balls on the WLCSP package (C5, D5, E4, E6, F5, F6, G4, G5, H5) can be left floating or can be connected to VSSC or VSSO.

Ezairo 8300 DIO Assignment

Some of the DIOs of Ezairo 8300 have a default assignment to a given interface, as shown in the table below.

DIOs: DEFAULT ASSIGNMENT

VDDO1	VDDO2	VDDO3	VDDO4
DIO0: SPI_CLK; EMMC_CLK	DIO12: Unassigned	DIO24: Unassigned	DIO30: SW_TCK (**)
DIO1: SPI_CS; EMMC_CMD	DIO13: Unassigned	DIO25: Unassigned	DIO31: SW_TMS (**)
DIO2: SPI_IO0; EMMC_DATA0	DIO14: Unassigned	DIO26: Unassigned	DIO32: JTDI (**)
DIO3: SPI_IO1	DIO15: Unassigned	DIO27: Unassigned	DIO33: JTDO (**)
DIO4: Unassigned	DIO16: Unassigned	DIO28: Unassigned	DIO34: Unassigned
DIO5: Unassigned	DIO17: Unassigned	DIO29: Unassigned	DIO35: Unassigned (***)
DIO6: Unassigned	DIO18: Unassigned		
DIO7: Unassigned	DIO19: Unassigned		
DIO8: Unassigned (*)	DIO20: Unassigned (*)		
DIO9: Unassigned (*)	DIO21: Unassigned (*)		
DIO10: Unassigned (*)	DIO22: Unassigned (*)		
DIO11: Unassigned (*)	DIO23: Unassigned (*)		

*LSAD capability: this functionality is not available on other DIOs.
**SWJ−DP capability: this functionality is not available on other DIOs.
***EXTCLK capability: this functionality is not available on other DIOs.

Ezairo 8300 Passive Components

The following 7 capacitors are mandatory:

MANDATORY CAPACITORS

Cap (VBAT − VSSC)	VBAT decoupling	1 μF	±20%
Cap (VBATOD − VSSOD)	VBATOD decoupling	4.7 μF	±20%
Cap (VDDC − VSSC)	VDDC decoupling	100 nF	±20%
Cap (VDDM − VSSC)	VDDM decoupling	100 nF	±20%
Cap (VDDA − VSSA)	VDDA decoupling	2.2 μF	±20%
Cap (VDDA_C0 − VDDA_C1)	Analog charge pump	100 nF (Note 16)	±20%
Cap (VREG − VSSA)	VREG decoupling	1 μF	±20%

16. The startup current limit can be increased with a higher capacitor value. Recommended maximum value is 470 nF.

Depending on the amount of current and the current profile needed by an external IC, VDDA can be used to supply this IC, and VDDIF is not needed. This will be the case for an external device that requires a low and constant current to operate.

Some use cases will require the usage of VDDIF, for example when a radio system is used. When VDDIF is used, the following 2 capacitors are needed:

VDDIF CAPACITORS

Cap (VDDIF_C0- VDDIF_C1)	Interfaces charge pump	0.47 μF	±20%
Cap (VDDIF–VSSO)	VDDIF decoupling	2.2 μF	±20%

Special care is needed at the system level to avoid audio artefacts.

The VDDO supplies need decoupling capacitors if the supplies are not derived from VBAT, VDDA, or VDDIF (all of which are already decoupled). This adds up to 4 optional capacitors:

VDDOX CAPACITORS

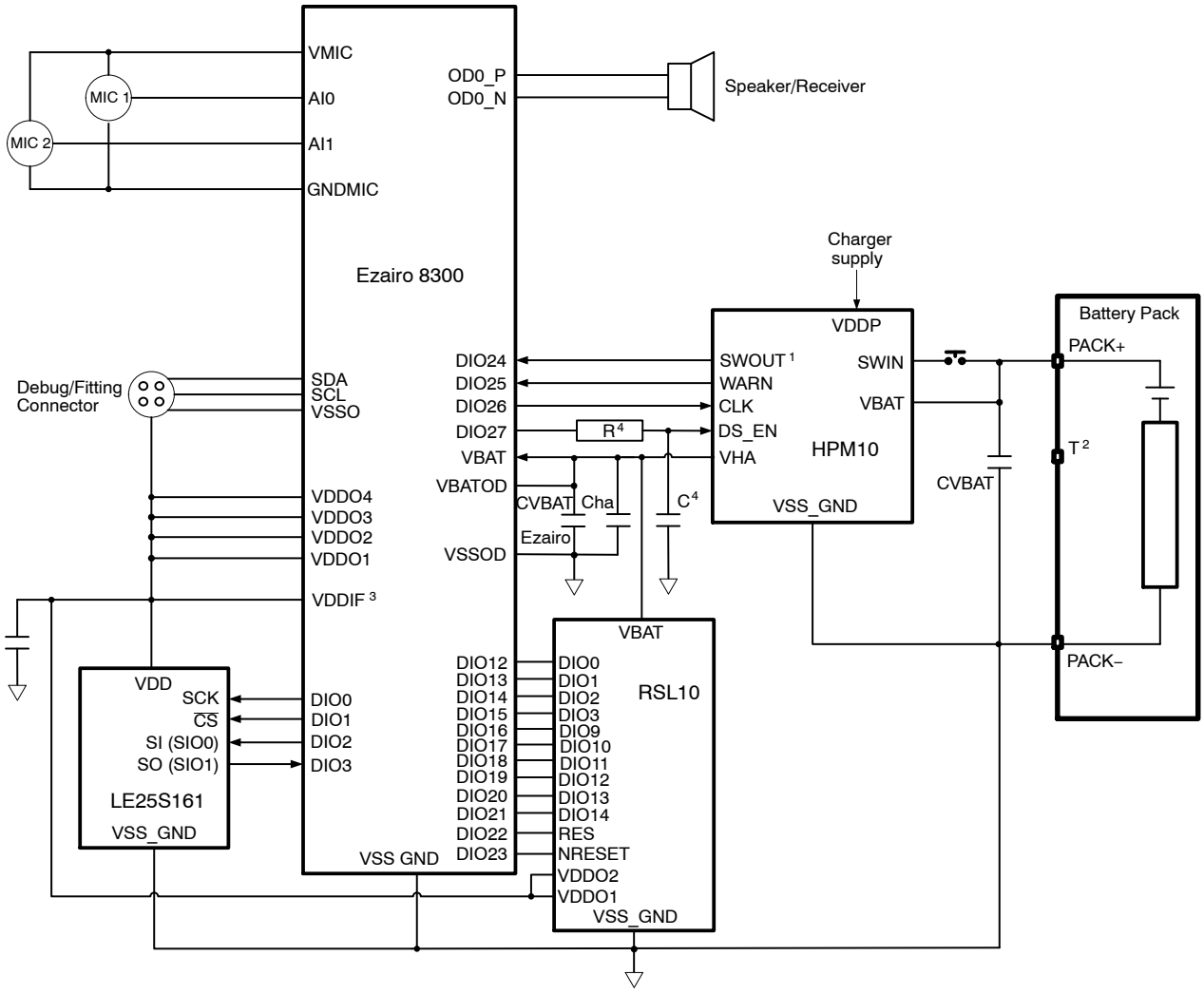
Cap (VDDO1–VSSO)	VDDO1 decoupling	2.2 μF	±20%
Cap (VDDO2– VSSO)	VDDO2 decoupling	2.2 μF	±20%
Cap (VDDO3– VSSO)	VDDO3 decoupling	2.2 μF	±20%
Cap (VDDO4– VSSO)	VDDO4 decoupling	2.2 μF	±20%

A cap on VMIC will be used if the VMIC regulator is used:

Cap (VMIC–VSSA)	VMIC decoupling	1 μF	±20%

A DC blocking capacitor on the analog input for microphone signal can be added in designs that operate with MEMS microphones powered by approximately 0.9 – 1.3 V with an output bias point of approximately Vdd/2 (0.45 V–0.65 V):

CAP (MIC output – AIX)	DC blocking capacitors on analog inputs	100 nF	±20%



Notes:
1. SWIN, SWOUT, WARN and CLK are optional (design dependant)
2. The Thermistor in the battery pack may be connected to a LSAD input of the Ezairo 8300 SL for A/D conversion using the voltage divider.
3. If any of the VDDO* domains on Ezairo 8300 are not referenced to VDDIF or VBAT, they require a 2.2 uF decoupling capacitor.
4. Recommended component values for the RC filter and required DIO configuration:
    a. R = 3K9 ohm, 1%; C = 0.56 uF, 10%
    b. RC filter should be driven by a VBAT DIO from Ezairo with strong pull up, i.e. 1 Kohm
5. Cha is the decoupling capacitor for VHA and should be placed next to the VHA pad.
6. CVBAT is the decoupling capacitor for the battery and its value should always be 5*(Cha+CVBAT Ezairo)
7. Details of the capacitor selection for Cha and other capacitors not shown on this diagram for HPM10 can be found in «External Components» Section of the HPM10 datasheet
8. Details of the decoupling capacitor selection for Ezairo can be found at section «Ezairo 8300 Passive Components»
9. Please contact **onsemi** for a review of your schematics.

Figure 5. Ezairo 8300 Application Diagram

BUMP AND COATING SPECIFICATIONS

Subject	Specification
Bump metallization	SnAg (Ag = 1.8%)
Backside coating specification	Lintec Adwill 2850
Backside coating thickness	25 μm

Chip Identification

System identification is used to identify different system components. For the Ezairo 8300 chip, the key identifier components and values are as follows:

- Chip Family: 0x0A
- Chip Version: 0x01
- Chip Revision: 0x0101

Electrostatic Discharge (ESD) Sensitive Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

Inspection Criteria

MIL−STD−883 Method 2010 is followed.

Solder Information

The Ezairo 8300 chip, WLCSP version, is delivered solder bumped, constructed with all RoHS compliant material and should be reflowed accordingly.

The Ezairo 8300 VFBGA package is constructed with all RoHS compliant material and should be reflowed accordingly.

The WLCSP version is Moisture Sensitive Class MSL1 and the VFBGA version has been classified as Moisture Sensitive Class MSL3 according to IPC/JEDEC standard J−STD−020E, Joint Industry Standard: Re−flow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. Handle parts according to J−STD−033D, Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture, Reflow and Process Sensitive Devices. Hand soldering is not recommended for this part.

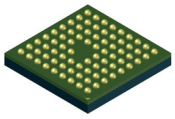
For additional information on our Pb−free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Company or Product Inquiries

For more information about **onsemi** products or services visit our Web site at http://onsemi.com.

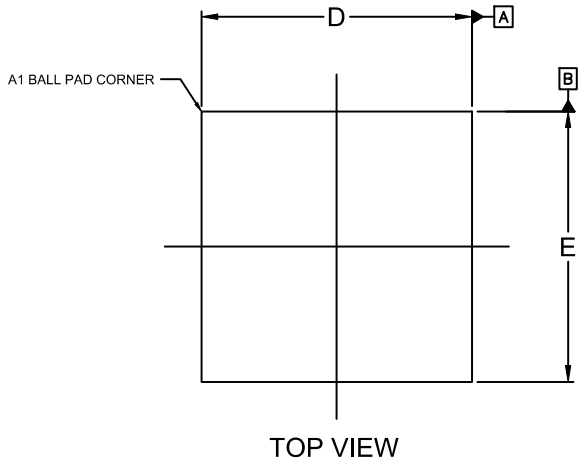
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VFBGA78 5x5
CASE 138AW
ISSUE B

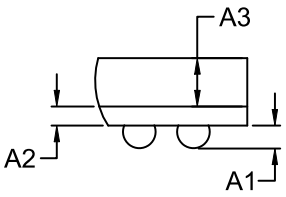
DATE 14 MAY 2020



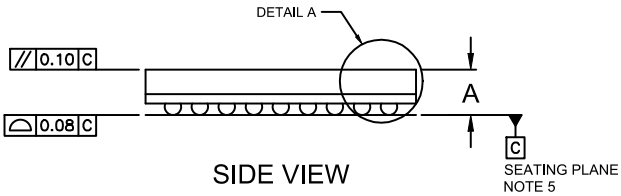
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

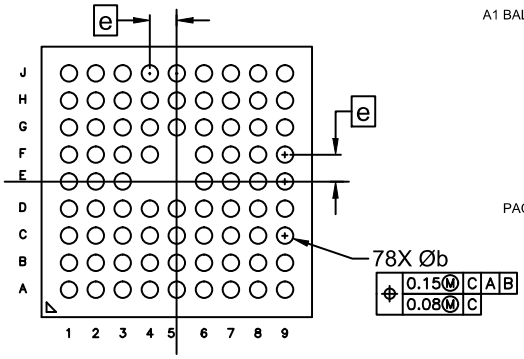
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	MIN.	NOM.	MAX.
A	---	---	0.983
A1	0.16	---	0.26
A2	0.242 REF		
A3	0.450 REF		
b	0.27	---	0.37
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.50 BSC		



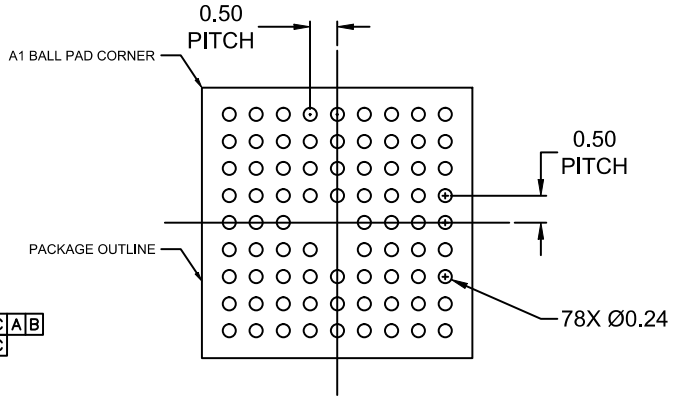
DETAIL A



SIDE VIEW



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



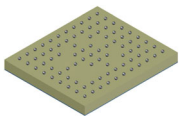
XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
CCC = Country of Origin
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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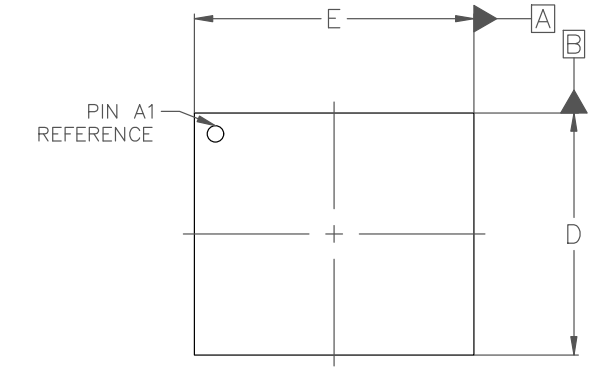
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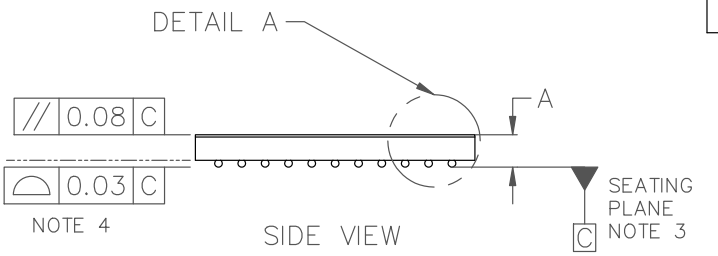


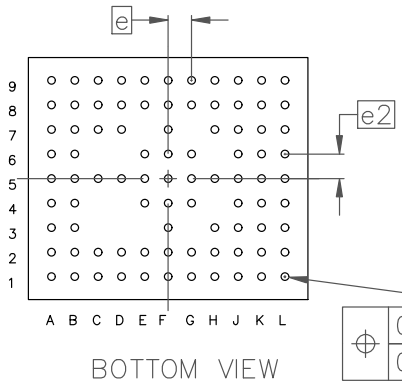
WLCSP−87 2.643x3.053x0.354, 0.255P
CASE 567ZN
ISSUE D

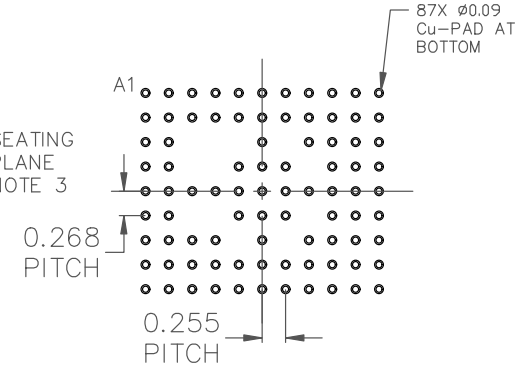
DATE 19 OCT 2026



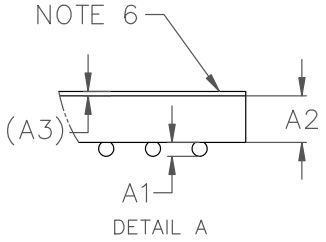
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	MIN.	NOM.	MAX.
A	0.329	0.354	0.379
A1	0.060	0.075	0.090
A2	0.241	0.254	0.267
A3		0.025 REF	
b	0.087	0.102	0.117
D	2.593	2.643	2.693
E	3.003	3.053	3.103
e		0.255 BSC	
e2		0.268 BSC	







RECOMMENDED
MOUNTING FOOTPRINT
(NSMD PAD TYPE)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.
6. BACKSIDE COATING.

GENERIC
MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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DESCRIPTION:	**WLCSP−87 2.643x3.053x0.354, 0.255P**		**PAGE 1 OF 1**

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