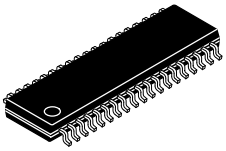
CM2031

HDMI Receiver Port Protection and Interface Device



ON Semiconductor®

http://onsemi.com



TSSOP 38
TR SUFFIX
CASE 948AG

MARKING DIAGRAM

CM2031−A0TR

CM2031−A0TR = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
CM2031−A0TR	TSSOP−38 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Product Description

The CM2031 HDMI Receiver Port Protection and Interface Device is specifically designed for next generation HDMI Sink interface protection.

An integrated package provides all ESD, level shifting/isolation and backdrive protection for an HDMI port in a single 38−Pin TSSOP package.

CM2031 is ideal for applications which do not require HDMI certification but can benefit from level shifters and backdrive protection.

Features

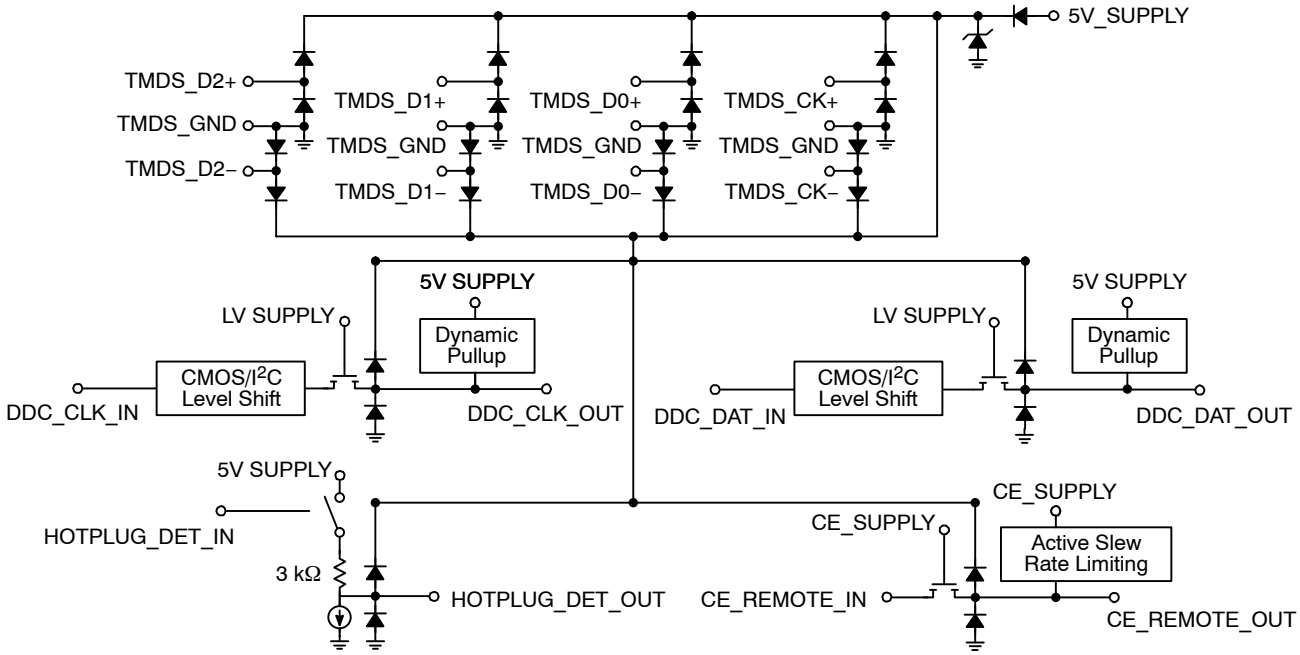
- Supports Thin Dielectric and 2−layer Boards
- Minimizes TMDS Skew with 0.05 pF Matching
- Long HDMI Cable Support with Integrated I^2C Accelerator
- Supports Direct Connection to CEC Microcontroller
- Integrated I^2C Level Shifting to CMOS Level Including Low Logic Level Voltages
- Integrated ±8 kV ESD Protection and Backdrive Protection on All External I/O Lines
- Supports Active and Passive Control of Hot Plug Detect Signal
- Multiport I^2C Support Eliminates Need for Analog Mux on DDC Lines
- Simplified Layout with Matched 0.5 mm Trace Spacing
- These Devices are Pb−Free and are RoHS Compliant

Applications

- PC and Consumer Electronics
- Digital TV, PC Monitors and Projectors

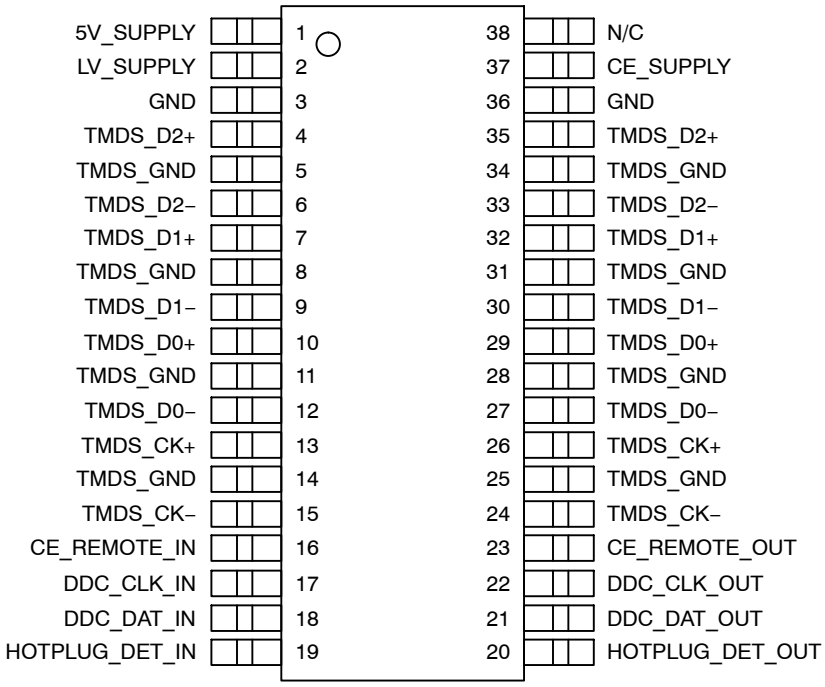
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ELECTRICAL SCHEMATIC



PACKAGE / PINOUT DIAGRAM

Top View



38−Pin TSSOP Package

Table 1. PIN DESCRIPTIONS

Pins	Name	ESD Level	Description
4, 35	TMDS_D2+	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
6, 33	TMDS_D2−	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
7, 32	TMDS_D1+	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
9, 30	TMDS_D1−	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
10, 29	TMDS_D0+	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
12, 27	TMDS_D0−	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
13, 26	TMDS_CK+	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
15, 24	TMDS_CK−	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
16	CE_REMOTE_IN	2 kV (Note 4)	CE_SUPPLY Referenced Logic Level In
23	CE_REMOTE_OUT	8 kV(Note 3)	5V_SUPPLY Referenced Logic Level Out plus 10 pF ESD
17	DDC_CLK_IN	2 kV (Note 4)	LV_SUPPLY Referenced Logic Level In
22	DDC_CLK_OUT	8 kV (Note 3)	5V_SUPPLY Referenced Logic Level Out plus 10 pF ESD
18	DDC_DAT_IN	2 kV (Note 4)	LV_SUPPLY Referenced Logic Level In
21	DDC_DAT_OUT	8 kV (Note 3)	5V_SUPPLY Referenced Logic Level Out plus 10 pF ESD
19	HOTPLUG_DET_IN	2 kV (Note 4)	LV_SUPPLY Referenced Logic Level In
20	HOTPLUG_DET_OUT	8 kV (Note 3)	5V_SUPPLY Referenced Logic Level Out plus 10 pF ESD. A 0.1 μF Bypass Ceramic Capacitor is Recommended on this Pin (Note 2).
2	LV_SUPPLY	2 kV (Note 4)	Bias for CE / DDC / HOTPLUG Level Shifters
37	CE_SUPPLY	2 kV (Notes 2 & 4)	CEC Bias Voltage. Previously CM2020 ESD_BYP Pin.
1	5V_SUPPLY	2 kV (Note 4)	Current Source for 5V_OUT, VREF for DDC I^2C Voltage References, and Bias for 8 kV ESD Pins.
38	N/C	N/A	N/C
3, 5, 8, 11, 14, 25, 28, 31, 34, 36	GND / TMDS_GND	N/A	GND Reference

1. These 2 pins need to be connected together in−line on the PCB. See recommended layout diagram.
2. This output can be connected to an external 0.1 μF ceramic capacitor/pads to maintain backward compatibility with the CM2020.
3. Standard IEC 61000−4−2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, 5V_OUT (pin 38), and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1 μF ceramic capacitor connected to GND.
4. Human Body Model per MIL−STD−883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, 5V_OUT (pin 38), and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1 μF ceramic capacitor connected to GND.
5. These pins should be routed directly to the associated GND pins on the HDMI connector with single point ground vias at the connector.

BACKDRIVE PROTECTION AND ISOLATION

Backdrive current is defined as the undesirable current flow through an I/O pin when that I/O pin's voltage exceeds the related local supply voltage for that circuitry. This is a potentially common occurrence in multimedia entertainment systems with multiple components and several power plane domains in each system.

For example, if a DVD player is switched off and an HDMI connected TV is powered on, there is a possibility of reverse current flow back into the main power supply rail of the DVD player from pull−ups in the TV. As little as a few milliamps of backdrive current flowing back into the power rail can charge the DVD player's bulk bypass capacitance on the power rail to some intermediate level. If this level rises above the power−on−reset (POR) voltage level of some of the integrated circuits in the DVD player, then these devices may not reset properly when the DVD player is turned back on.

If any SOC devices are incorporated in the design which have built−in level shifter and/or ESD protection structures, there can be a risk of permanent damage due to backdrive. In this case, backdrive current can forward bias the on−chip ESD protection structure. If the current flow is high enough, even as little as a few milliamps, it could destroy one of the SOC chip's internal DRC diodes, as they are not designed for passing DC.

To avoid either of these situations, the CM2031 was designed to block backdrive current, guaranteeing less than 5 μA into any I/O pin when the I/O pin voltage exceeds its related operating CM2031 supply voltage.

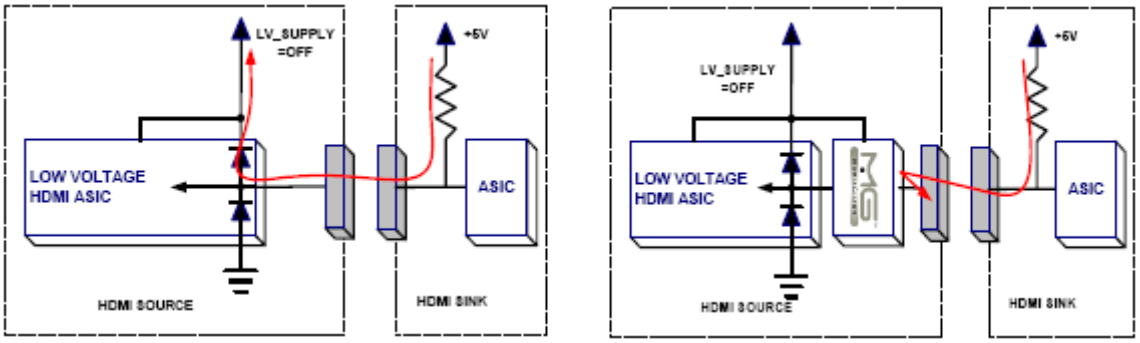


Figure 1. Backdrive Protection Diagram.

DISPLAY DATA CHANNEL (DDC) LINES

The DDC interface is based on the I^2C serial bus protocol for EDID configuration.

Dynamic Pullups

Based on the HDMI specification, the maximum capacitance of the DDC line can approach 800 pF (50 pF from source, 50 pF from sink, and 700 pF from cable). At the upper range of capacitance values (i.e. long cables), it becomes impossible for the DDC lines to meet the I^2C timing specifications with the minimum pull−up resistor of 1.5 kΩ (at the source).

For this reason, the CM2031 was designed with an internal I^2C accelerator to meet the AC timing specification even with very long and non−compliant cables.

The internal accelerator works with the source pull−up and the local 47 kΩ pullup to increase the positive slew rate of the DDC_CLK_OUT and DDC_DAT_OUT lines whenever the sensed voltage level exceeds 0.3*5V_SUPPLY (approximately 1.5 V). This provides faster overall risetime in heavily loaded situations without overloading the mutli−drop open drain I^2C outputs elsewhere.

Figure 2 demonstrates the "worst case" operation of the dynamic CM2031 DDC level shifting circuitry (bottom) against a discrete NFET common−gate level shifter circuit with a typical 1.5 kΩ pullup at the source (top.) Both are shown driving an off−spec, but unfortunately readily available 31 m HDMI cable which exceeds the 700 pF HDMI specification. Some widely available HDMI cables have been measured at *over 4 nF.*

When the standard I/OD cell releases the NFET discrete shifter, the risetime is limited by the pullup and the parasitics of the cable, source and sink. For long cables, this can extend the risetime and reduce the margin for reading a valid "high" level on the data line. In this case, an HDMI source may not be able to read uncorrupted data and will not be able to initiate a link.

With the CM2031's dynamic pullups, when the ASIC driver releases its DDC line and the "OUT" line reaches at least 0.3*VDD (of 5V_SUPPLY), then the "OUT" active pullups are enabled and the CM2031 takes over driving the cable until the "OUT" voltage approaches the 5V_SUPPLY rail.

The internal pass element and the dynamic pullups also work together to damp reflections on the longer cables and keep them from glitching the local ASIC.

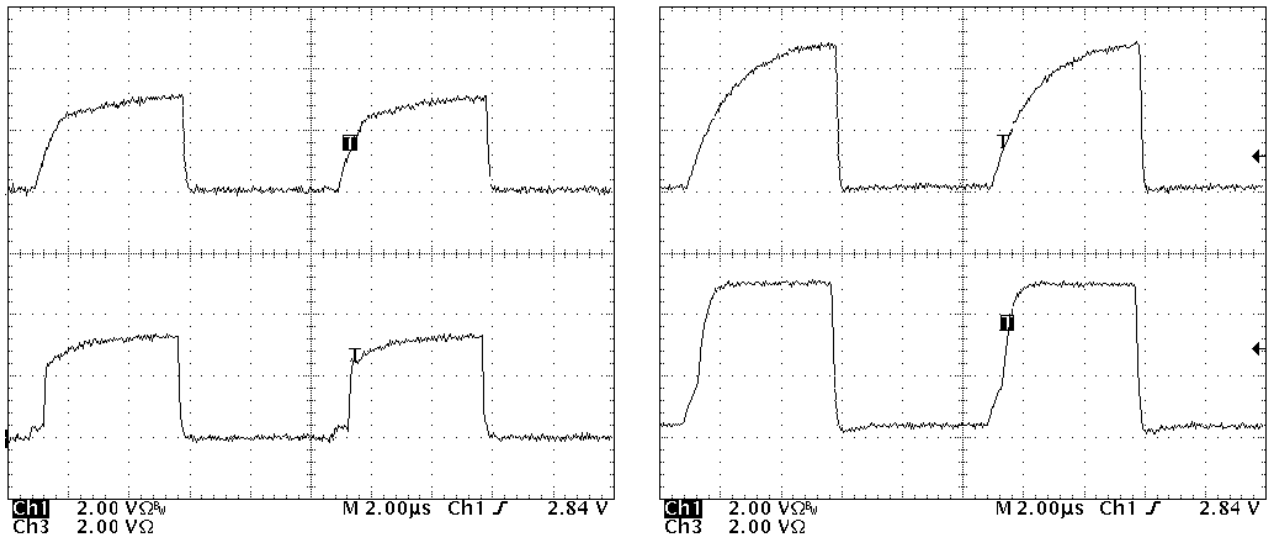


Figure 2. Dynamic DDC Pullups
(Discrete − Top, CM2031 − Bottom; 3.3 V ASIC − Left, 5 V Cable − Right)

I²C Low Level Shifting

In addition to the Dynamic Pullups described in the previous section, then CM2031 also incorporates improved I²C low−level shifting on the DDC_CLK_IN and DDC_DAT_IN lines for enhanced compatibility.

Typical discrete NFET level shifters can advertise specifications for low R_{DS}[on], but usually state relatively high $V_{[GS]}$ test parameters, requiring a 'switch' signal (gate voltage) as high as 10 V or more. At a sink current of 4 mA for the ASIC on DDC_XX_IN, the CM2031 guarantees no more than 140 mV increase to DDC_XX_OUT, even with a switching control of 2.5 V on LV_SUPPLY.

Additionally, when I²C devices are driving the external cable, an internal pulldown on DDC_XX_IN guarantees that the VOL seen by the ASIC on DDC_XX_IN is equal to or lower than DDC_XX_OUT.

Multiport DDC Multiplexing

Additionally, by switching LV_SUPPLY, the DDC/HPD blocks can be independently disabled by engaging their inherent "backdrive" protection. This allows N:1 multiplexing of the low−speed HDMI signals without any additional FET switches.

CONSUMER ELECTRONICS CONTROL (CEC)

The Consumer Electronics Control (CEC) line is a high level command and control protocol, based on a single wire multidrop open drain communication bus running at approximately 1 kHz (See Figure 3). While the HDMI link provides only a single point−to−point connection, up to ten (10) CEC devices may reside on the bus, and they may be daisy chained out through other physical connectors including other HDMI ports or other dedicated CEC links. The high level protocol of CEC can be implemented in a simple microcontroller or other interface with any I/OD (input/open−drain) GPIO.

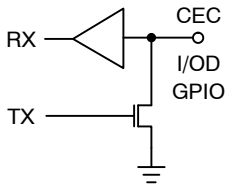


Figure 3. Typical µC I/OD Driver

To limit possible EMI and ringing in this potentially complex connection topology, the rise− and fall−time of this line are limited by the specification. However, meeting the slew−rate limiting requirements with additional discrete circuitry in this bi−directional block is not trivial without an additional RX/TX control line to limit the output slew−rate without affecting the input sensing (See Figure 4).

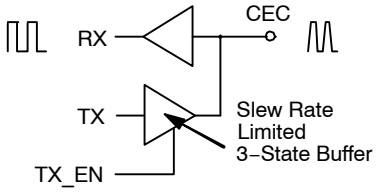


Figure 4. Three−Pin External Buffer Control

Simple CMOS buffers cannot be used in this application since the load can vary so much (total pullup of 27 kΩ to less than 2 kΩ, and up to 7.3 nF total capacitance.) The CM2031 targets an output drive slew−rate of less than 100 mV/μs regardless of static load for the CEC line. Additionally, the same internal circuitry will perform active termination, thus reducing ringing and overshoot in entertainment systems connected to legacy or poorly designed CEC nodes.

The CM2031's bi−directional slew rate limiting is integrated into the CEC level−shifter functionality thus allowing the designer to directly interface a simple low voltage CMOS GPIO directly to the CEC bus and simultaneously guarantee meeting all CEC output logic levels and HDMI slew−rate and isolation specifications (See Figure 5).

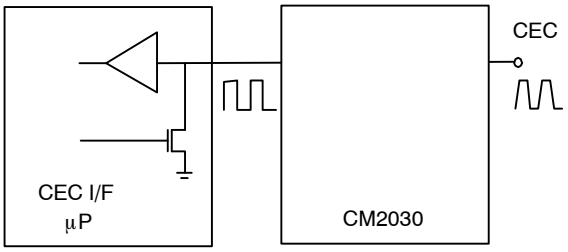


Figure 5. Integrated CM2031 Solution

The CM2031 also includes an internal backdrive protected static pullup 120 μA current source from the CE_SUPPLY rail in addition to the dynamic slew rate control circuitry.

Figure 6 shows a typical shaped CM2031 CEC output (bottom) against a ringing uncontrolled discrete solution (top).

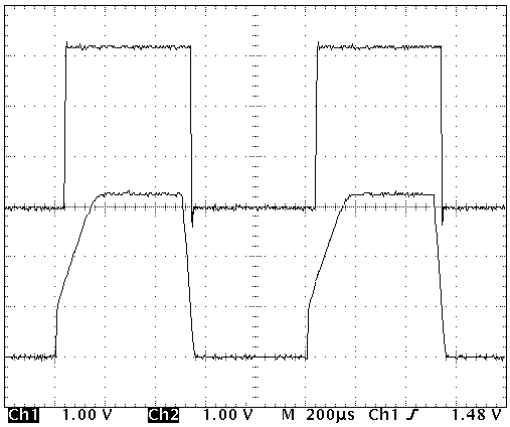


Figure 6. CM2031 CEC Output

HDMI certification requires capacitance measurement of the CEC line to be less than 150 pF per device. Due to the active circuit inside the CM2031 CEC line, CM2031 may cause false readings during the CEC capacitance measurement and not pass the test. The active circuit of the CM2031 CEC line would react with the LCR meter and cause false capacitance readings. There is no issue with the operation of the CM2031 CEC line during normal operations. In fact, CM2031 CEC has shown to improve the signal integrity of the CEC line. CM2031 can be used for applications which do not require HDMI certification or applications which do not use the CEC line.

HOTPLUG OUTPUT PULLUP LOGIC

The CM2031 includes flexible circuitry for active or passive control of the HDMI Sink's Hotplug Present Output line by integrating the 1 kΩ pullup resistor.

Section 8.5 of the HDMI Specification allows the HDMI Sink to pulse the HotPlug line "low" for at least 100 msec to indicate to the Source that the EEPROM should be re−read. This function can be implemented with a few discrete components as shown in Figure 7.

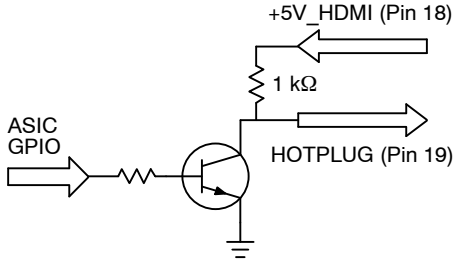


Figure 7. Typical Discrete HPD Switching Circuit

The Hot Plug Detect circuit of the CM2031 is specifically designed to provide this "pulse" capability and still pass CTS testing requirements.

When a logic "high" is applied to the HOTPLUG_DET_IN pin, an internal switch enables the 1 kΩ pull−up. When a logic "low" is sensed on this pin, the 1 kΩ logic resistor is disconnected, and a weak pulldown ensures a valid low output on the HDMI cable.

5 V Passive Pullup

In the most basic implementation, where HOTPLUG is to be asserted only when the HDMI +5 V supply is applied, simply tie HOTPLUG_DET_IN to the +5 V supply and connect HOTPLUG_DET_OUT to HDMI Connector (Pin 19).

Local Power Supply Pullup Passive

For a system that needs to inhibit the HOTPLUG signal when the local ASIC low voltage supply ("LV_SUPPLY" on CM2031) has been powered, the designer can simply

connect HOTPLUG_DET_OUT to the HDMI Connector (Pin 19) and tie HOTPLUG_DET_IN to the “LV_SUPPLY” which can be 1.5 V, 1.8 V, 2.5 V, etc. Then the internal 1 kΩ pullup will be enabled between HOTPLUG_DET_OUT and 5V_SUPPLY.

If a weak pullup is used on HOTPLUG_DET _IN, then this still allows dynamic switching by the local ASIC while still retaining the isolation/backdrive protection on this pin.

Active Local Pullup Control

For a system where a low voltage GPIO signal needs to control the HOTPLUG pin (i.e. if the local system needs to boot up before asserting HOTPLUG) the ASIC GPIO can be connected directly to the HOTPLUG_DET_IN pin to control the 5 V pullup “on” and “off.” A logic “low” on HOTPLUG_DET_IN will disable the 5 V pullup, and a logic “high” will enable the pullup.

NOTE: If the ASIC Power−ON Reset {POR} default of the GPIO is high−impedance or defaults to an input, then the designer should include a weak pulldown on the GPIO to eliminate any POR glitches.

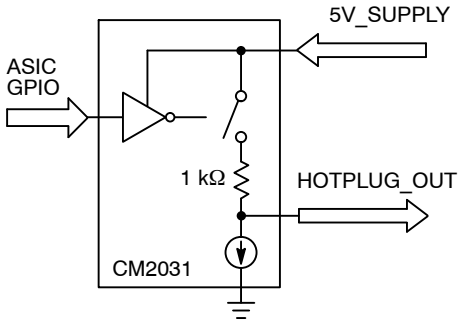


Figure 8. Simplified CM2031 HPD Circuit

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
V_{CC5}, V_{CCLV}	6.0	V
DC Voltage at any Channel Input	[GND − 0.5] to [VCC + 0.5]	V
Storage Temperature Range	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD (RECOMMENDED) OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
5V_SUPPLY	Operating Supply Voltage	−	5.0	5.5	V
LV_SUPPLY	Bias Supply Voltage	1.0	3.3	5.5	V
CE_SUPPLY	Bias Supply Voltage	3.0	3.3	3.6	V
−	Operating Temperature Range	−40	−	85	°C

SPECIFICATIONS (Cont'd)

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC5}	Operating Supply Current	5V_SUPPLY = 5.0 V, CEC_OUT = 3.3 V, LV_SUPPLY = 3.3 V, CE_SUPPLY = 3.3 V, DDC = 5 V (Note 11)		300	350	μA
I_{CCLV}	Bias Supply Current	LV_SUPPLY = 3.3 V (Note 12)		60	150	μA
I_{CCCE}	Bias Supply Current	CE_SUPPLY = 3.3 V, CEC_OUT = 0 V (Notes 11 and 12)		60	150	μA
I_{CEC}	Current Source on CEC Pin	CE_SUPPLY = 3.3 V	111	120	128	μA
I_{OFF}	OFF State Leakage Current, Level Shifting NFET	LV_SUPPLY = 0 V (Note 7) HOTPLUG_IN = 0 V		0.1	5	μA
$I_{BACKDRIVE}$, TMDS	Current Through TMDS Pins when Powered Down	All Supplies = 0 V, TMDS_[2:0]+/, TMDS_CK+/ = 4 V		0.1	5	μA
$I_{BACKDRIVE}$, DDC	Current Through DDC_DAT_OUT when Powered Down	All Supplies = 0 V, DDC_DAT/CLK_OUT = 5 V, DDC_DAT/CLK_IN = 0 V		0.1	5	μA
$I_{BACKDRIVE}$, HOTPLUG	Current Through HOTPLUG_DET_OUT when Powered Down	All Supplies = 0 V, HOTPLUG_DET_OUT = 5 V, HOTPLUG_IN = 0 V		0.1	5	μA
$I_{BACKDRIVE}$, CEC	Current Through CE_REMOTE_OUT when Powered Down	CE_REMOTE_IN = CE_SUPPLY < CE_REMOTE_OUT		0.1	1.8	μA
CEC_{SL}	CEC Slew Limit	Measured from 10−90% or 90−10%		0.26	0.65	V/μs
CEC_{RT}	CEC Rise Time	Measured from 10−90% Assumes a signal swing from 0−3.3 V	26.4		250	μs
CEC_{FT}	CEC Fall Time	Measured from 90−10% Assumes a signal swing from 0−3.3 V	4		50	μs
$R_{HOTPLUG}$	Hotplug Resistance	Voltage on HotPlug_In is greater than the specified range below	0.8	1.0	1.2	kΩ
V_{TH}	Threshold Voltage to Assert 1 kΩ		1.5		5.5	V
V_{ACC}	Turn On Threshold of I^2C / DDC Accelerator	Voltage is 0.3 X 5 V_Supply (Note 7)	1.35	1.5	1.65	V
$V_{ON(DDC_OUT)}$	Voltage Drop across DDC Level Shifter	LV_SUPPLY = 3.3 V, 3 mA Sink at DDC_{IN}, $DDC_{OUT} < V_{ACC}$		150	225	mV
$V_{OL(DDC_IN)}$	Logic Level (ASIC side) when I^2C / DDC Logic Low Applied (I^2C Pass−through Compatibility)	DDC_OUT = 0.4 V, LV_SUPPLY = 3.3 V, 1.5 kΩ Pullup on DDC_OUT to 5.0 V		0.3	0.4	V
$tr_{(DDC)}$	DDC_OUT Line Risetime, $V_{ACC} < V_{DDC_OUT} <$ (5V_Supply − 0.5 V)	DDC_IN floating, LV_SUPPLY = 3.3 V, 1.5 kΩ pullup on DDC_OUT to 5.0 V, Bus Capacitance = 1500 pF			1	μs
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8 mA, T_A = 25°C (Note 7)	 0.6 0.6	 0.85 0.85	 0.95 0.95	V
V_{ESD}	ESD Withstand Voltage (IEC)	Pins 4, 7, 10, 13, 20, 21, 22, 23, 24, 27, 30, 33, T_A = 25°C (Note 7)	±8			kV

6. Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
7. Standard IEC61000−4−2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY = 5 V, 3.3V_SUPPLY = 3.3 V, LV_SUPPLY = 3.3 V, GND = 0 V.
8. Human Body Model per MIL−STD−883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ, 5V_SUPPLY = 5V, 3.3V_SUPPLY = 3.3 V, LV_SUPPLY = 3.3 V, GND = 0 V.
9. Intra−pair matching, each TMDS pair (i.e. D+, D−)
10. These measurements performed with no external capacitor on V_P (V_P floating)
11. These static measurements do not include AC activity on controlled I/O lines.
12. This measurement does not inclue supply current for the 120 μA current source on the CEC pin.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ESD}	ESD Withstand Voltage (HBM)	Pins 1, 2, 16, 17, 18, 19, 37, 38, T_A = 25°C (Note 8)	±2			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1 A, t_P = 8/20 μS (Note 10)		 11.0 2.0		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1 A, t_P = 8/20 μS Any I/O pin to Ground (Note 10)		 1.4 0.9		Ω
I_{LEAK}	TMDS Channel Leakage Current	T_A = 25°C		0.01	1	μA
C_{IN}, TMDS	TMDS Channel Input Capacitance	5V_SUPPLY = 5.0 V, Measured at 1 MHz, V_{BIAS} = 2.5 V		0.9	1.2	pF
ΔC_{IN}, TMDS	TMDS Channel Input Capacitance Matching	5V_SUPPLY = 5.0 V, Measured at 1 MHz, V_{BIAS} = 2.5 V (Note 9)		0.05		pF
C_{MUTUAL}	Mutual Capacitance between Signal Pin and Adjacent Signal Pin	5V_SUPPLY = 0 V, Measured at 1 MHz, V_{BIAS} = 2.5 V		0.07		pF
C_{IN}, DDC_{OUT}	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY = 0 V, Measured at 100 kHz, V_{BIAS} = 2.5 V		10		pF
C_{IN}, CEC_{OUT}	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY = 0 V, Measured at 100 kHz, V_{BIAS} = 1.65 V		10		pF
C_{IN}, HP_{OUT}	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY = 0 V, Measured at 100 kHz, V_{BIAS} = 2.5 V (Note 7)		10		pF

6. Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
7. Standard IEC61000−4−2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY = 5 V, 3.3V_SUPPLY = 3.3 V, LV_SUPPLY = 3.3 V, GND = 0 V.
8. Human Body Model per MIL−STD−883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ, 5V_SUPPLY = 5V, 3.3V_SUPPLY = 3.3 V, LV_SUPPLY = 3.3 V, GND = 0 V.
9. Intra−pair matching, each TMDS pair (i.e. D+, D−)
10. These measurements performed with no external capacitor on V_P (V_P floating)
11. These static measurements do not include AC activity on controlled I/O lines.
12. This measurement does not inclue supply current for the 120 μA current source on the CEC pin.

PERFORMANCE INFORMATION

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

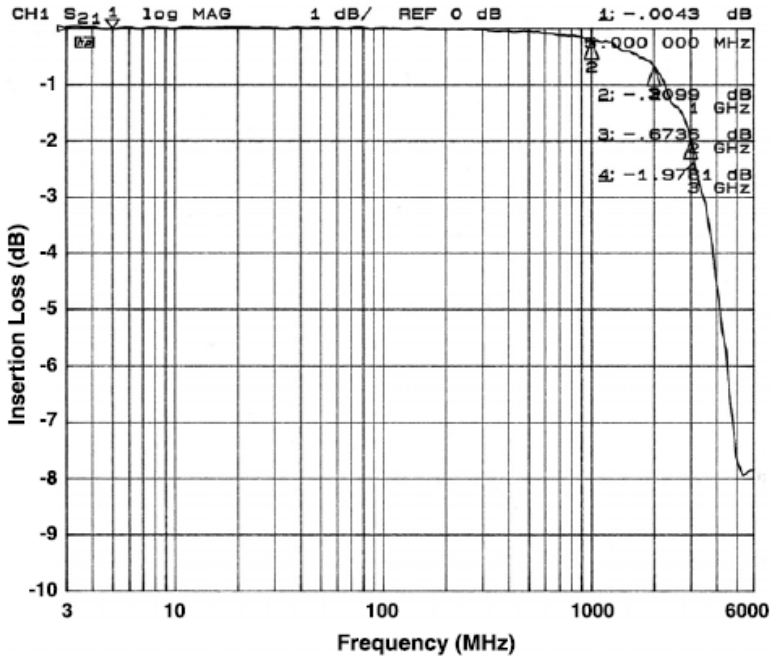


Figure 9. Insertion Loss vs. Frequency (TMDS_D1− to GND)

APPLICATION INFORMATION

Design Considerations

DUT On vs. DUT Off

Many HDMI CTS tests require a power off condition on the System Under Test. Many discrete ESD diode configurations can be forward biased when their VDD rail is lower than the I/O pin bias, thereby exhibiting extremely high apparent capacitance measurements, for example. The *MediaGuard*™ backdrive isolation circuitry limits this current to less than 5 μA, and will help ensure HDMI compliance.

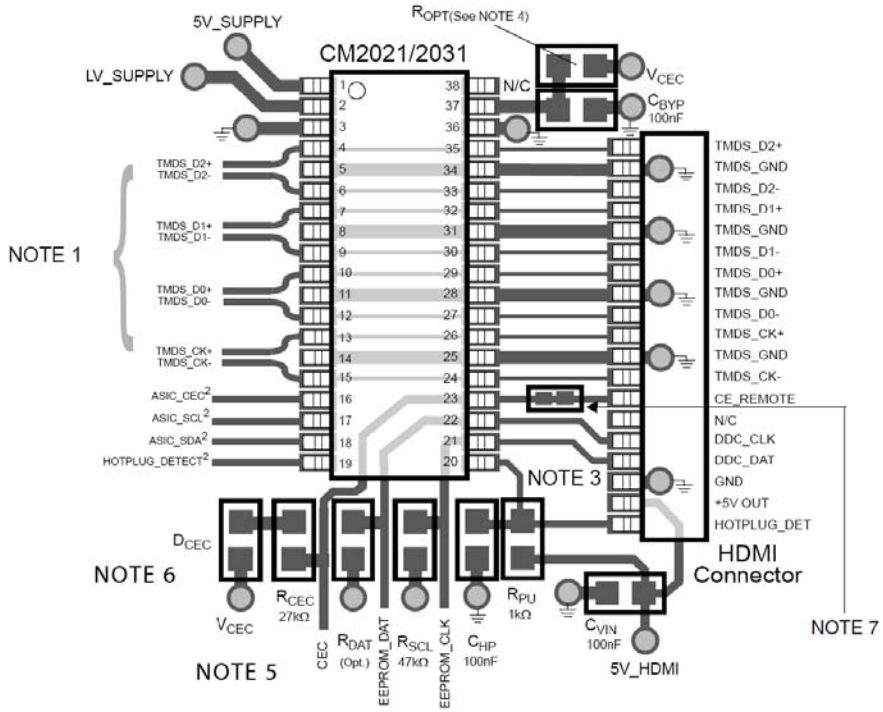


Figure 10. Typical Application for CM2031

Layout Notes

1. Differential TMDS Pairs should be designed as normal 100 Ω HDMI Microstrip. *Single Ended (decoupled) TMDS traces underneath MediaGuard™, and traces between MediaGuard™* and Connector should be tuned to match chip/connector IBIS parasitics. (See *MediaGuard™* Layout Application Notes.)
2. Level Shifter signals should be biased with a weak pullup to the desired local LV_SUPPLY. If the local ASIC includes sufficient pullups to register a logic high, then external pullups may not be needed.
3. Place MediaGuard™ as close to the connector as possible, and as with any controlled impedance line always avoid placing any silkscreen printing over TMDS traces.
4. CM2021/CM2031 footprint compatibility − For the CM2031, Pin 37 becomes the V_{CEC} power supply pin for the slew−rate limiting circuitry. This can be supplied by a 0 Ω jumper to V_{CEC} which should be depopulated to utilize the CM2021. The 100 nF C_{BYP} is recommended for all applications.
5. CEC pullup isolation − The 27 k R_{CEC} and a Schottky D_{CEC} provide the necessary isolation for the CEC pullup.

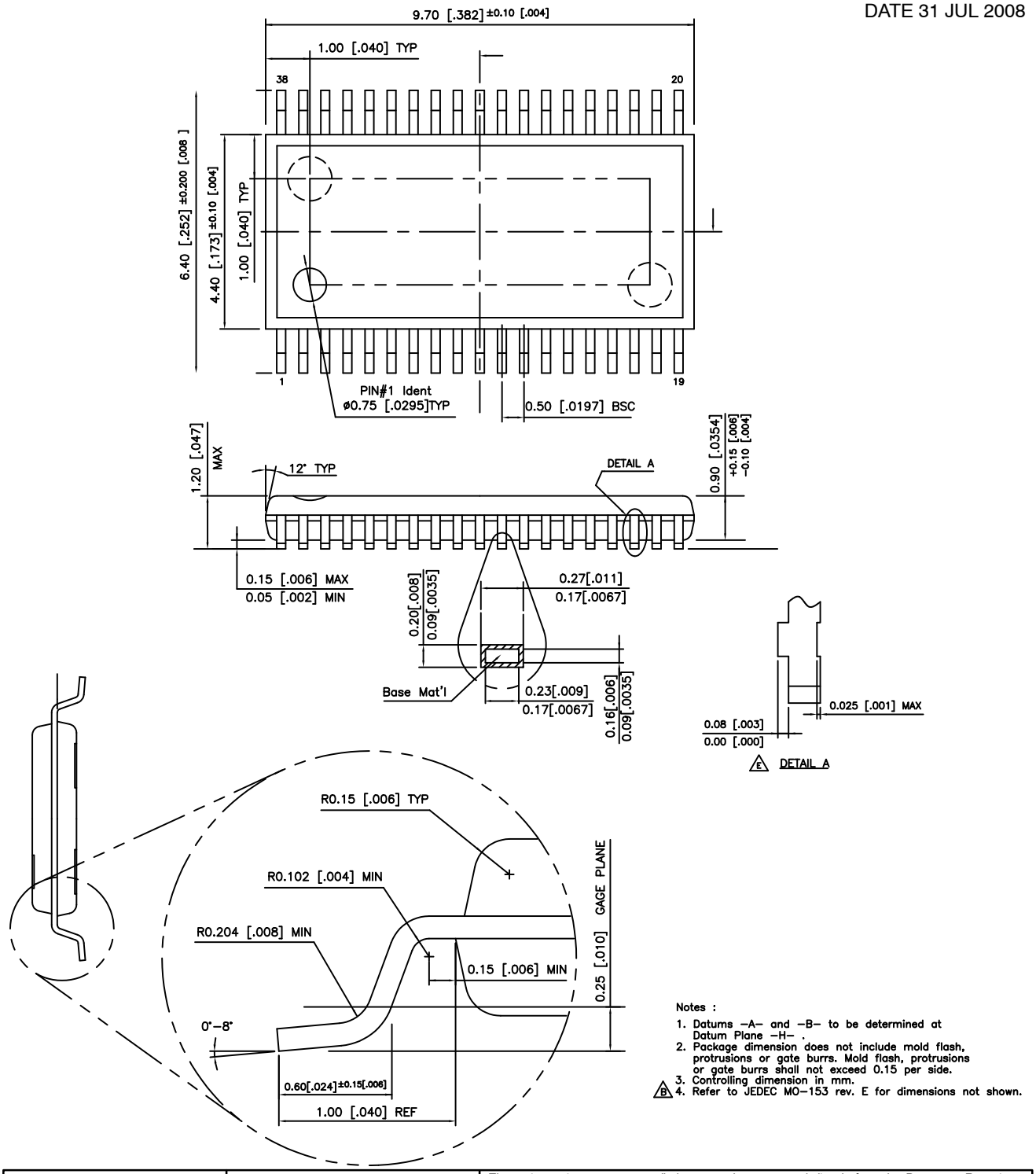
NOTE: *This circuitry is used only in the CM2021.* Depopulate the components for CM2031 applications in a CM2021/CM2031 dual footprint layout.

6. Footprint compatibility − The CM2031 has (built−in) internal backdrive protection. The CM2021 does not not have internal backdrive protection and requires the external R_{CEC} and D_{CEC} components.
7. (For CM2031) If CEC firmware *is not* implemented, *do not* populate with 0 Ω resistor. If CEC firmware is implemented, then populate with 0 Ω resistor.
   (For CM2021) Populate with 0 Ω resistor in either case.

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Notes :
1. Datums −A− and −B− to be determined at Datum Plane −H− .
2. Package dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
3. Controlling dimension in mm.
B 4. Refer to JEDEC MO−153 rev. E for dimensions not shown.

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