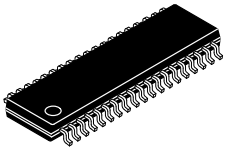
CM2020-00TR

HDMI Transmitter Port Protection and Interface Device

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TSSOP 38
TR SUFFIX
CASE 948AG

Product Description

The CM2020−00TR HDMI Transmitter Port Protection and Interface device is specifically designed for next generation HDMI source interface protection.

An integrated package provides all ESD, level shift, overcurrent output protection and backdrive protection for an HDMI port in a single 38−Pin TSSOP package.

The CM2020−00TR part is specifically designed to complement the CM2021 protection part in HDMI receivers (Displays, DTV, CE devices, etc.)

The CM2020−00TR also incorporates a silicon overcurrent protection device for +5 V supply voltage output to the connector.

Features

- HDMI 1.3 Compliant
- 0.05 pF Matching Capacitance between the TMDS Intra−Pair
- Overcurrent Output Protection
- Level Shifting/Isolation Circuitry
- Provides ESD Protection to IEC61000−4−2 Level 4
  - 8 kV Contact Discharge
  - 15 kV Air Discharge
- Matched 0.5 mm Trace Spacing (TSSOP)
- Simplified Layout for HDMI Connectors
- Backdrive Protection
- These Devices are Pb−Free and are RoHS Compliant

Applications

- PC
- Consumer Electronics
- Set Top Box
- DVDRW Players

MARKING DIAGRAM

CM2020−00TR

CM2020−00TR = Specific Device Code

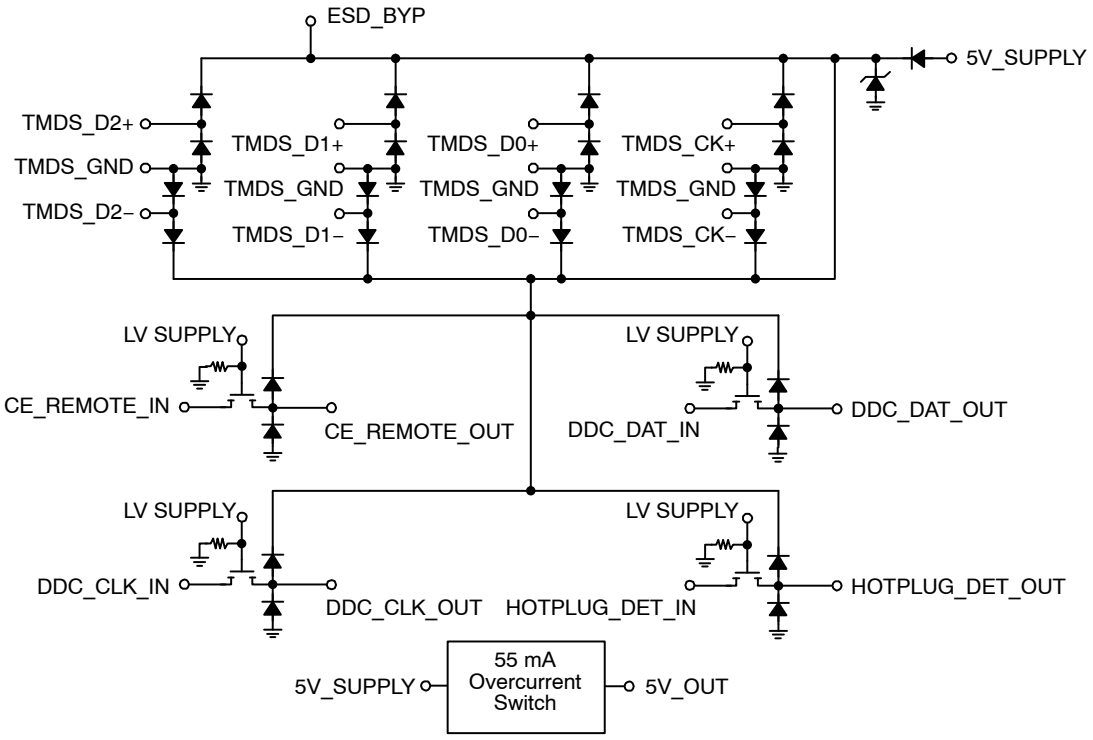
ORDERING INFORMATION

Device	Package	Shipping†
CM2020−00TR	TSSOP−38 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

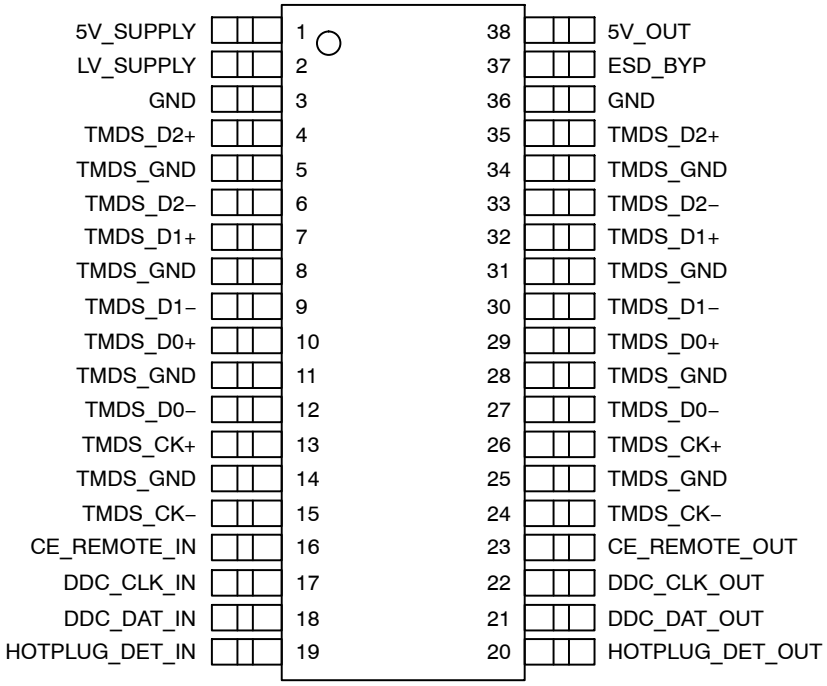
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ELECTRICAL SCHEMATIC



PACKAGE / PINOUT DIAGRAM

Top View



38−Pin TSSOP Package

Table 1. PIN DESCRIPTIONS

Pins	Name	ESD Level	Description
4, 35	TMDS_D2+	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
6, 33	TMDS_D2−	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
7, 32	TMDS_D1+	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
9, 30	TMDS_D1−	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
10, 29	TMDS_D0+	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
12, 27	TMDS_D0−	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
13, 26	TMDS_CK+	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
15, 24	TMDS_CK−	8 kV (Note 3)	TMDS 0.9 pF ESD Protection (Note 1)
16	CE_REMOTE_IN	2 kV (Note 4)	LV_SUPPLY Referenced Logic Level into ASIC
23	CE_REMOTE_OUT	8 kV(Note 3)	5V_SUPPLY Referenced Logic Level Out plus 3.5 pF ESD to Connector
17	DDC_CLK_IN	2 kV (Note 4)	LV_SUPPLY Referenced Logic Level into ASIC
22	DDC_CLK_OUT	8 kV (Note 3)	5V_SUPPLY Referenced Logic Level Out plus 3.5 pF ESD to Connector
18	DDC_DAT_IN	2 kV (Note 4)	LV_SUPPLY Referenced Logic Level into ASIC
21	DDC_DAT_OUT	8 kV (Note 3)	5V_SUPPLY Referenced Logic Level Out plus 3.5 pF ESD to Connector
19	HOTPLUG_DET_IN	2 kV (Note 4)	LV_SUPPLY Referenced Logic Level into ASIC
20	HOTPLUG_DET_OUT	8 kV (Note 3)	5V_SUPPLY Referenced Logic Level Out plus 3.5 pF ESD (Note 2) to Connector
2	LV_SUPPLY	2 kV (Note 4)	Bias for CE / DDC / HOTPLUG Level Shifters
1	5V_SUPPLY	2 kV (Note 4)	Current Source for 5V_OUT
38	5V_OUT	8 kV (Note 3)	55 mA Minimum Overcurrent Protected 5 V Output. This Output Must be Bypassed with a 0.1 μF Ceramic Capacitor.
37	ESD_BYP	2 kV (Note 4)	This Pin must be Connected to a 0.1 μF Ceramic Capacitor
3, 36	GND	N/A	Supply GND Reference
5, 34, 8, 31, 11, 28, 14, 25	TMDS_GND	N/A	TMDS ESD and Parasitic GND Return (Note 5)

1. These 2 pins need to be connected together in−line on the PCB.
2. This output can be connected to an external 0.1 μF ceramic capacitor, resulting in an increased ESD withstand voltage rating.
3. Standard IEC 61000−4−2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V and ESD_BYP (pin 37), 5V_OUT (pin 38), and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1 μF ceramic capacitor connected to GND.
4. Human Body Model per MIL−STD−883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V and ESD_BYP (pin 37), 5V_OUT (pin 38), and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1 μF ceramic capacitor connected to GND.
5. These pins should be routed directly to the associated GND pins on the HDMI connector with single point ground vias at the connector.

BACKDRIVE PROTECTION

Below, two scenarios are discussed to illustrate what can happen when a powered device is connected to an unpowered device via a HDMI interface, substantiating the need for backdrive protection on this type of interface.

In the first example a DVD player is connected to a TV via an HDMI interface. If the DVD player is switched off and the TV is left on, there is a possibility of reverse current flow back into the main power supply rail of the DVD player. Typically, the DVD's power supply has some form of bulk supply capacitance associated with it. Because all CMOS logic exhibits a very high impedance on the power rail node when "off", if there may be very little parasitic shunt resistance, and even with as little as a few milliamps of "backdrive" current flowing into the power rail, it is possible over time to charge that bulk supply capacitance to some intermediate level. If this level rises above the power−on−reset (POR) voltage level of some of the integrated circuits in the DVD player, these devices may not reset properly when the DVD player is turned back on.

In a more serious scenario, if any SOC devices are incorporated in the design which have built−in level shifter and DRC diodes for ESD protection, there is even a risk for permanent damage. In this case, if there is a pullup resistor (such as with DDC) on the other end of the cable, then that resistance will pull the SOC chips "output" up to a high level. This will forward bias the upper ESD diode in the DRC and charge the bulk capacitance in a similar fashion as described in the first example. If this current flow is high enough, even as little as a few milliamps, it could destroy one of the SOC chip's internal DRC diodes, as they are not designed for passing DC.

To avoid either of these situations, the CM2020−00TR was designed to block backdrive current, guaranteeing no more than 5 mA on any I/O pin when the I/O pin voltage is greater than the CM2020−00TR supply voltage.

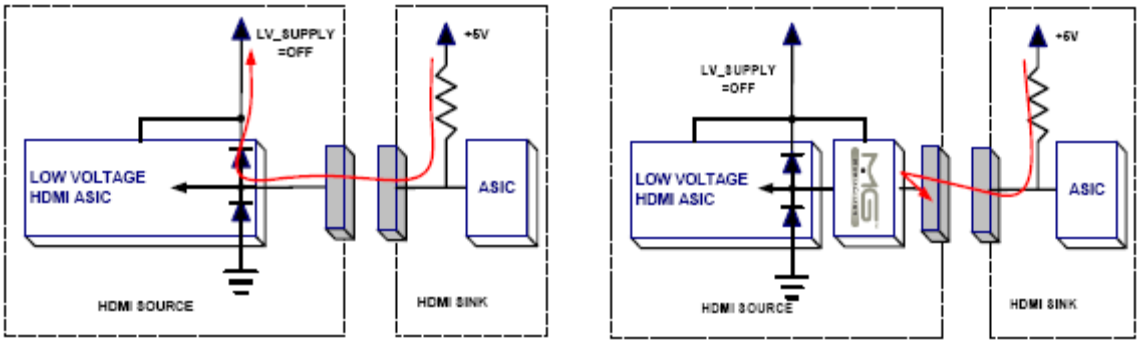


Figure 1. Backdrive Protection Diagram.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
V_{CC5V}, V_{CCLV}	6.0	V
DC Voltage at any Channel Input	6.0	V
Storage Temperature Range	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD (RECOMMENDED) OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
5V_SUPPLY	Operating Supply Voltage	GND	5	5.5	V
LV_SUPPLY	Bias Supply Voltage	1	3.3	5.5	V
−	Operating Temperature Range	−40	−	85	°C

SPECIFICATIONS (Cont'd)

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC5V}	Operating Supply Current	5V_SUPPLY = 5.0 V		110	130	μA
I_{CCLV}	Bias Supply Current	LV_SUPPLY = 3.3 V		1	5	μA
V_{DROP}	5V_OUT Overcurrent Output Drop	5V_SUPPLY = 5.0 V, I_{OUT} = 55 mA		65	100	mV
I_{SC}	5V_OUT Short Circuit Current Limit	5V_SUPPLY = 5.0 V, 5V_OUT = GND	90	135	175	mA
I_{OFF}	OFF State Leakage Current, Level Shifting NFET	LV_SUPPLY = 0 V		0.1	5.0	μA
$I_{BACKDRIVE}$	Current Conducted from Output Pins to V_SUPPLY Rails when Powered Down	5V_SUPPLY < V_{CH_OUT} Signal Pins: TMDS_D[2:0]+/−, TMDS_CK+/−, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT, 5V_OUT Only		0.1	5.0	μA
$I_{BACKDRIVE, CEC}$	Current through CE−REMOTE_OUT when Powered Down	CE−REMOTE_IN = LV_SUPPLY < CE_REMOTE_OUT		0.1	1.0	μA
V_{ON}	VOLTAGE Drop Across Level Shifting NFET when ON	LV_SUPPLY = 2.5 V, V_S = GND, I_{DS} = 3 mA	75	95	140	mV
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8 mA, T_A = 25°C	 0.60 0.60	 0.85 0.85	 0.95 0.95	V
V_{ESD}	ESD Withstand Voltage, Contact Discharge per IEC 61000−4−2 Standard (IEC)	Pins 4, 7, 10, 13, 20, 21, 22, 23, 24, 27, 30, 33, 38; T_A = 25°C (Note 2)	±8			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1 A, t_P = 8/20 uS (Note 3)		 10.8 −2.1		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1 A, t_P = 8/20 μS, T_A = 25°C (Note 3)		 1.4 0.9		Ω
I_{LEAK}	TMDS Channel Leakage Current	T_A = 25°C		0.01	1	μA
$C_{IN, TMDS}$	TMDS Channel Input Capacitance	5V_SUPPLY = 5.0 V, Measured at 1 MHz, V_{BIAS} = 2.5 V		0.9	1.2	pF
$\Delta C_{IN, TMDS}$	TMDS Channel Input Capacitance Matching	5V_SUPPLY = 5.0 V, Measured at 1 MHz, V_{BIAS} = 2.5 V (Note 4)		0.05		pF
$C_{IN, DDC}$	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY = 5.0 V, Measured at 100 kHz, V_{BIAS} = 2.5 V (Note 2)		3.5	4	pF
$C_{IN, CEC}$	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY = 5.0 V, Measured at 100 kHz, V_{BIAS} = 2.5 V		3.5	4	pF
$C_{IN, HP}$	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY = 5.0 V, Measured at 100 kHz, V_{BIAS} = 2.5 V		3.5	4	pF

1. Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
2. Standard IEC 61000−4−2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V and ESD_BYP (pin 37), 5V_OUT (pin 38), and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1 μF ceramic capacitor connected to GND.
3. These measurements performed with no external capacitor on ESD_BYP.
4. Intra−pair matching, each TMDS pair (i.e. D+, D−).

PERFORMANCE INFORMATION

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

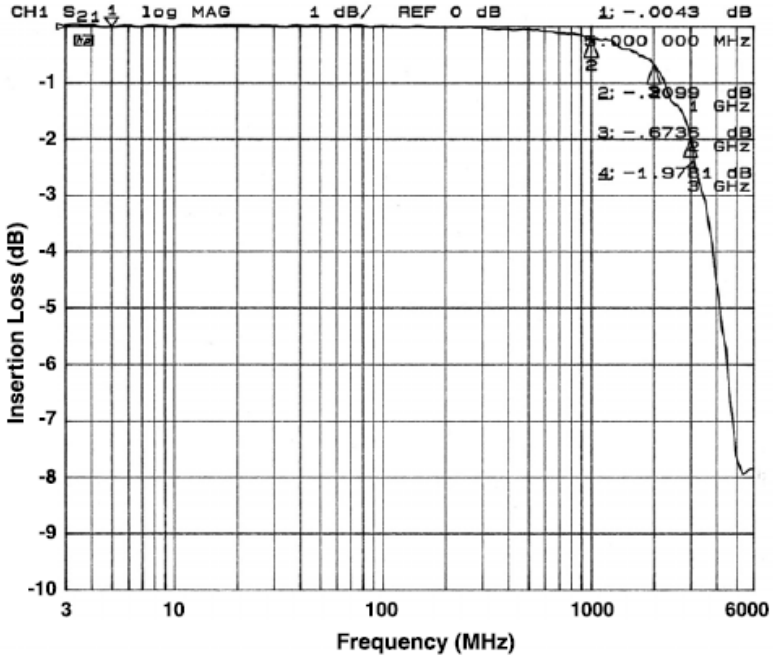
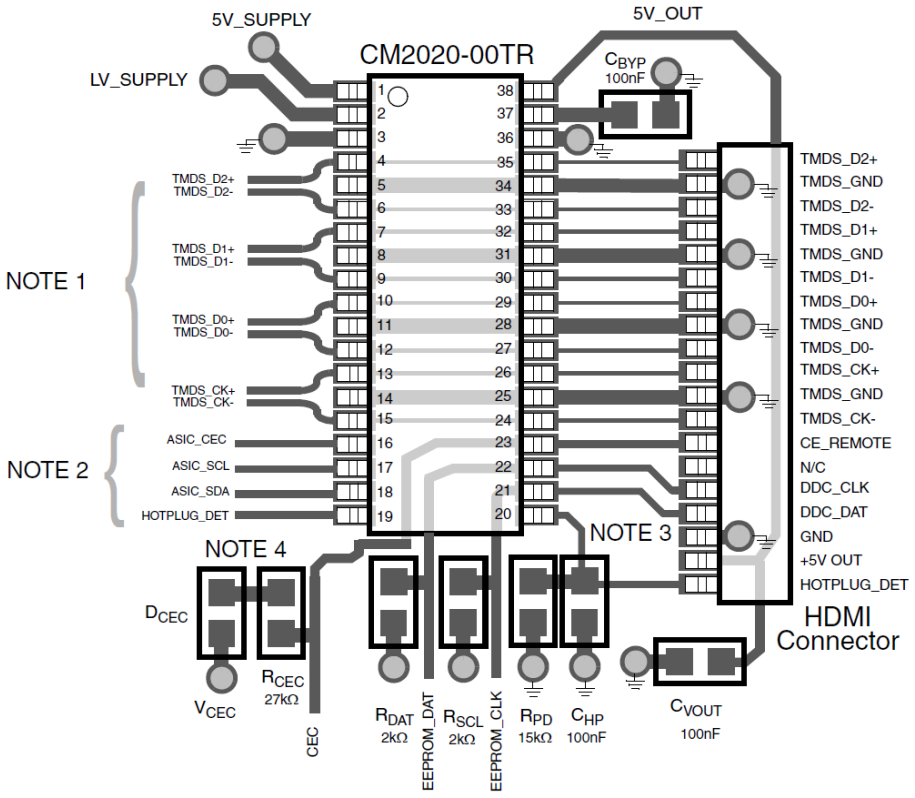


Figure 2. Insertion Loss vs. Frequency (TMDS_D1− to GND)

APPLICATION INFORMATION



LAYOUT NOTES

NOTE 1) Differential TMDS Pairs should be designed as normal 100W HDMI microstrip. Single Ended TMDS traces underneath CM2020 and between CM2020 and Connector should be tuned to match chip/connector parasitics. (See MediaGuard] Application Notes.)

NOTE 2) Level Shifter signals should be biased with a weak pullup to the desired local LV_SUPPLY. If the local ASIC includes sufficient pullups to register a logic high when the CM2020 NFET is “off”, then external pullups are not needed

NOTE 3) Place CM2020 as close to conector as possible, and as with any controlled impedance line avoid ANY silkscreening over TMDS lines.

NOTE 4) CEC pullup isolation. The 27k R_{CEC} and a Schottky D_{CEC} provide the necessary isolation for the CEC pullup.

Figure 3. Typical Application for CM2020−00TR

APPLICATION INFORMATION (Cont'd)

Design Considerations

ESD Bypass

Pin 37 (ESD_BYP) is provided for an optional external ESD bypass capacitor only (i.e. 0.1 μF ceramic). It should not be connected to any supply rail.

5V Overcurrent Output

Maximum Overcurrent Protection output drop at 55 mA on 5V_OUT is 100 mV. To meet HDMI output requirements of 4.8 − 5.3 V, an input of greater than 4.9 V should be used (i.e. 5.1 V ±4%). A 0.1 μF ceramic bypass capacitor on this output is also recommended.

Hotplug Detect Input

To meet the requirements of HDMI CTS TID7−12, the following pullup/pulldown configuration is recommended for a 3.3 V ±10% internal VCC rail (See Figure 4 below). A 0.1 μF ceramic capacitor is recommended for additional edge debounce and ESD bypass.

DUT On vs. DUT Off

Many HDMI CTS tests require a power off condition on the System Under Test. Many Dual Rail Clamp (DRC) ESD diode configurations will be forward biased when their VDD rail is lower than the I/O pin bias, thereby exhibiting extremely high apparent capacitance measurements, for example. The *MediaGuard*™ backdrive isolation circuitry limits this current to < 5 μA, and will help ensure compliance.

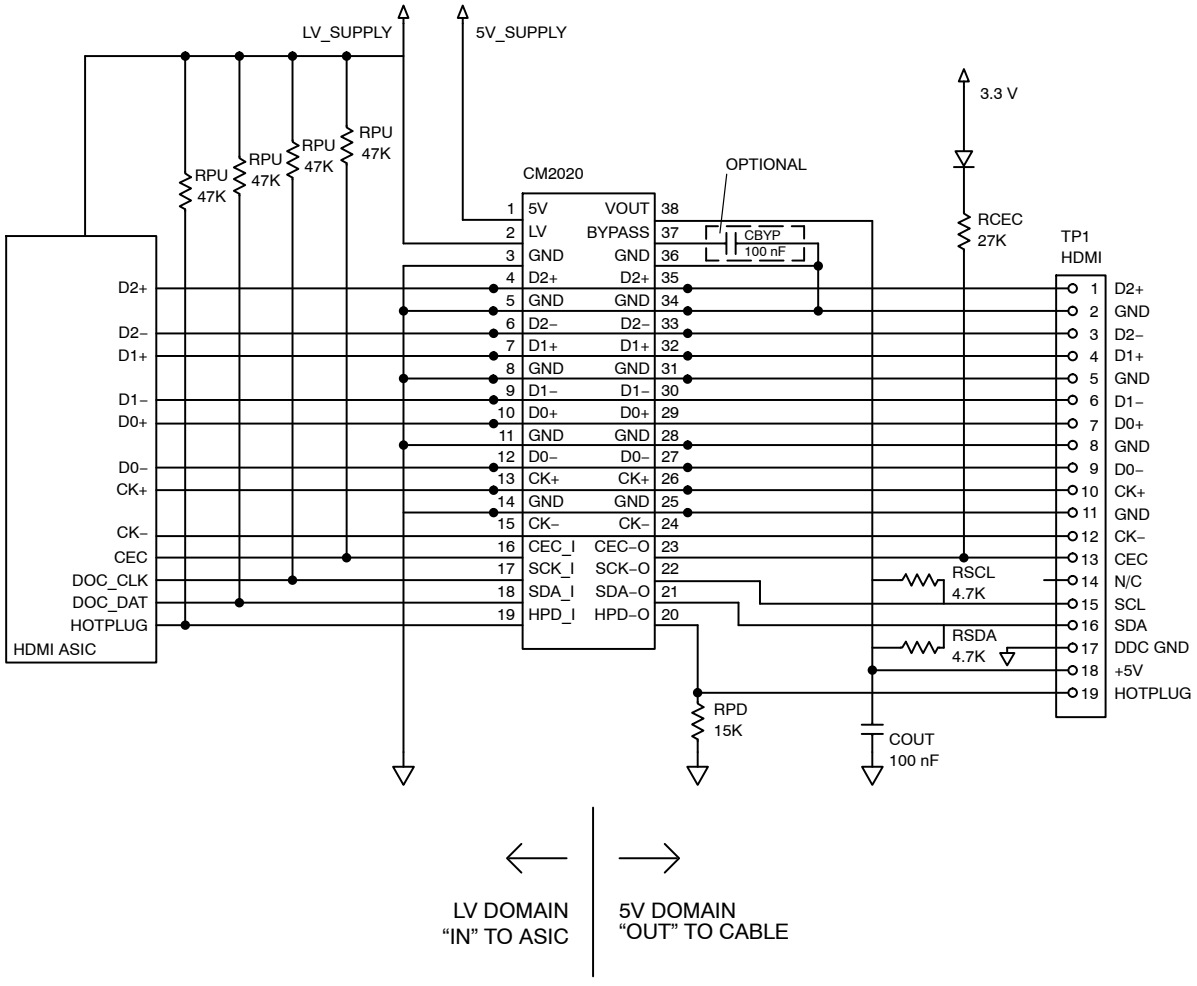
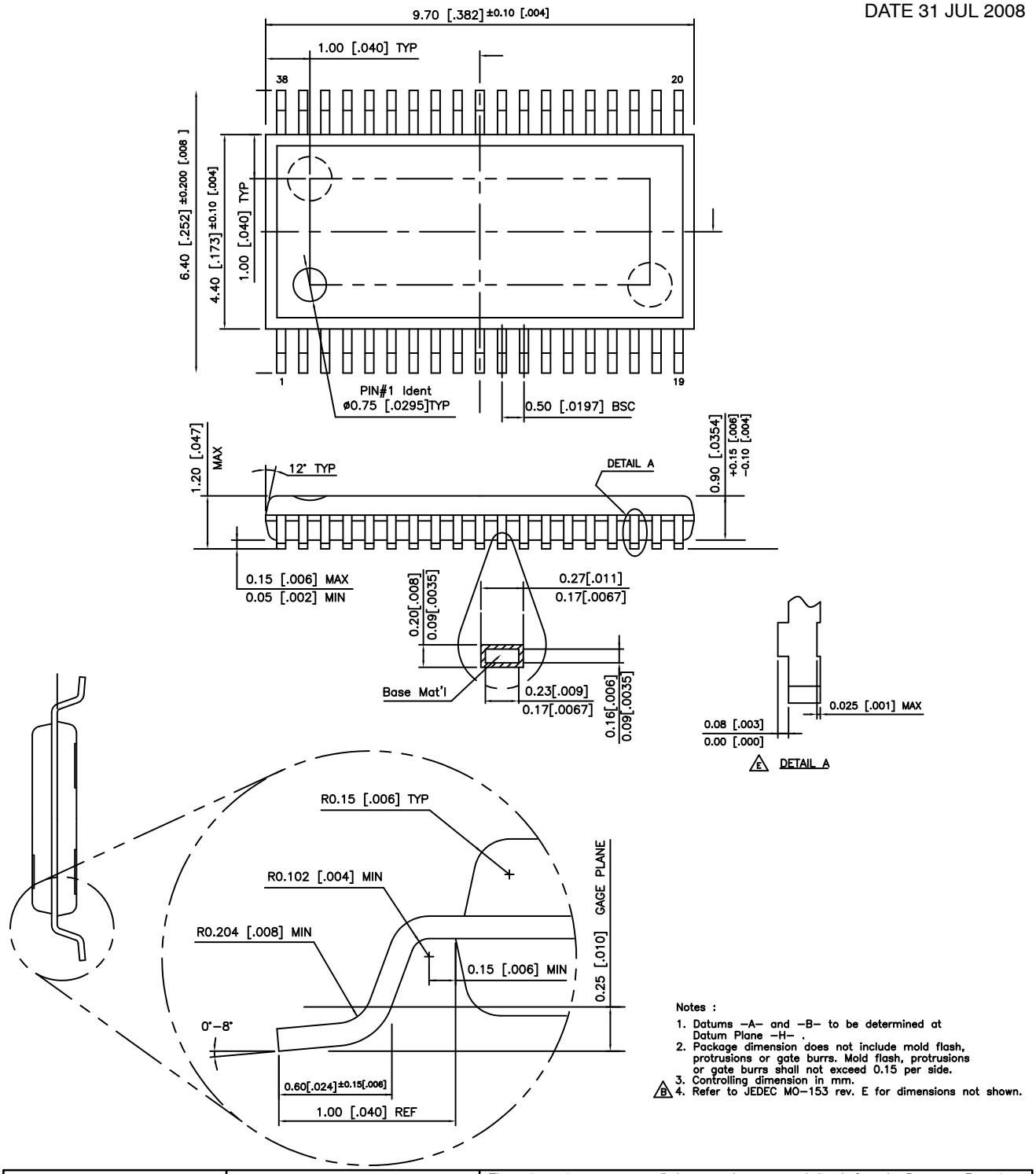


Figure 4. Design Example

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CASE 948AG
ISSUE O

DATE 31 JUL 2008



Notes :
1. Datums −A− and −B− to be determined at Datum Plane −H− .
2. Package dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
3. Controlling dimension in mm.
B 4. Refer to JEDEC MO−153 rev. E for dimensions not shown.

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