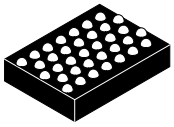
BelaSigna 300 with AfterMaster HD

Audio Processor for AfterMaster HD

ON Semiconductor®

www.onsemi.com



WLCSP−35
W SUFFIX
CASE 567AG

Introduction

BelaSigna® 300 AM is a DSP−based audio processor which is able to execute the AfterMaster HD algorithm within a system that also includes a host processor and/or external 12S− based mono or stereo A/D converters and D/A converters.

AfterMaster HD is an algorithm which processes audio signals in real−time to provide a significant increase in loudness, clarity, depth, and fullness.

BelaSigna 300 AM is specifically designed for use in applications requiring a solution to overcome the limitations of small or downward−facing speakers, including flat−screen televisions or headphones.

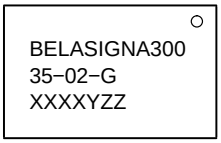
This datasheet describes only the specific information required to integrate BelaSigna 300 AM into an audio system.

For a more general description of the programmable BelaSigna 300 device from ON Semiconductor, please refer to the BelaSigna 300 datasheet.

Key Features

- **Ultra−low−power:** typically 4−8 mA when executing AfterMaster HD
- **Miniature Form Factor:** available in a miniature 3.63 mm x 2.68 mm x 0.92 mm (including solder balls) WLCSP package.
- **Full Range of Configurable Interfaces:** including a fast I^2C−based interface for download and general configuration of the AfterMaster HD algorithm, a highly configurable PCM interface to stream data into and out of the device, a high−speed UART, an SPI port and 5 GPIOs
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM



BELASIGNA300 = Device Code
35 = Number of Balls
02 = Revision of Die
G = Pb−Free
XXXX = Date Code
Y = Assembly Plant Identifier (May be Two Characters)
ZZ = Traceability Code

ORDERING INFORMATION

Device	Package	Shipping†
B300W35A109A1G	WLCSP (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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Figures and Data

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Voltage at any input pin	−0.3	2.0	V
Operating supply voltage (Note 1)	0.9	2.0	V
Operating temperature range (Note 2)	−40	85	°C
Storage temperature range	−55	85	°C
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V)			

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Functional operation only guaranteed below 0°C for digital core (VDDC) and system voltages above 1.0 V.
2. Parameters may exceed listed tolerances when out of the temperature range 0 to 50°C.

Electrical Performance Specifications

The tests were performed at 20°C with a clean 1.8 V supply voltage. BelaSigna 300 AM was running in high voltage mode (VDDC = 1.8 V unless otherwise noted). The system clock (SYS_CLK) was generated externally at 38 MHz.

Parameters marked as screened are tested on each chip. Other parameters are qualified but not tested on every part.

Table 2. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
OVERALL							
Supply voltage	V_{BAT}		1.8		2.0	V	√
Current consumption	I_{BAT}	AfterMaster HD @ Fs= 48 kHz	−	8	−	mA	√
		Fs = 44.1 kHz	−	7	−	mA	√
		Fs =16 kHz	−	3	−	mA	√
		Fs = 8 kHz	−	2	−	mA	
VREG (1 μF External Capacitor) Measurement at VDDC = 1.0 V, Low voltage mode							
Regulated voltage output	V_{REG}		0.95	1.00	1.05	V	√
Regulator PSRR	V_{REG_PSRR}	1 kHz	50	55	−	dB	
Load current	I_{LOAD}		−	−	2	mA	
Load regulation	$LOAD_{REG}$		−	6.1	6.5	mV/mA	√
Line regulation	$LINE_{REG}$		−	2	5	mV/V	
VDBL (1 μF External Capacitor) Measurement at VDDC = 1.0 V, Low voltage mode							
Regulated doubled voltage output	VDBL		1.9	2.0	2.1	V	√
Regulator PSRR	$VDBL_{PSRR}$	1 kHz	35	41	−	dB	
Load current	I_{LOAD}		−	−	2.5	mA	
Load regulation	$LOAD_{REG}$		−	7	10	mV/mA	√
Line regulation	$LINE_{REG}$		−	10	20	mV/V	
VDDC (1 μF External Capacitor) Measurement at VDDC = 1.0 V, Low voltage mode							
Digital supply voltage output	VDDC	Configured by a control register	0.79	0.95	1.25	V	√
VDDC output level adjustment	$VDDC_{STEP}$		27	29	31	mV	
Regulator PSRR	$VDDC_{PSRR}$	1 kHz	25	25.5	26	dB	
Load current	I_{LOAD}		−	−	3.5	mA	
Load regulation	$LOAD_{REG}$		−	3	12	mV/mA	√
Line regulation	$LINE_{REG}$		−	3	8	mV/V	

Table 2. ELECTRICAL SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
POWER−ON−RESET (POR)							
POR startup voltage	$VDDC_{STARTUP}$		0.775	0.803	0.837	V	
POR shutdown voltage	$VDDC_{SHUTDOWN}$		0.755	0.784	0.821	V	
POR hysteresis	$POR_{HYSTERESIS}$		13.8	19.1	22.0	mV	
POR duration	T_{POR}		11.0	11.6	12.3	ms	
DIGITAL PADS							
Voltage level for high input	V_{IH}		VBAT * 0.8	−	−	V	√
Voltage level for low input	V_{IL}		−	−	VBAT * 0.2	V	√
Voltage level for high output	V_{OH}	2 mA source current	VDDO * 0.8	−	−	V	√
Voltage level for low output	V_{OL}	2 mA sink current	−	−	VDDO * 0.2	V	√
Input capacitance for digital pads	C_{IN}		−	4	−	pF	
Pull−up resistance for digital input pads	R_{UP_IN}		220	270	320	kΩ	√
Pull−down resistance for digital input pads	R_{DOWN_IN}		220	270	320	kΩ	√
Sample rate tolerance	FS	Sample rate of 16 kHz or 32 kHz	−1	±0	+1	%	
Rise and fall time	Tr, Tf	Digital output pad					
ESD		Human Body Model (HBM)			2	kV	
		Machine Model (MM)			200	V	
Latch−up		V < GNDC, V > VBAT			200	mA	
DIGITAL INTERFACES							
I2C baud rate		System clock < 1.6 MHz	−	−	100	kbps	
		System clock > 1.6 MHz	−	−	400	kbps	
General−purpose UART baud rate		System clock ≥ 5.12 MHz	−	1	−	Mbps	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Environmental Characteristics

All BelaSigna 300 AM packages are Pb−free, RoHS−compliant and Green.

BelaSigna 300 AM parts are qualified against standards outlined in the following sections.

All BelaSigna 300 AM package options are Green (RoHS−compliant). Contact ON Semiconductor for supporting documentation.

WLCSP Package Option

The solder ball composition for the WLCSP package is SAC266.

Table 3. WLCSP PACKAGE−LEVEL QUALIFICATION

Packaging Level	
Moisture sensitivity level	JEDEC Level 1
Thermal cycling test (TCT)	−55°C to 150°C for 500 cycles
Highly accelerated stress test (HAST)	85°C / 85% RH for 1000 hours
High temperature stress test (HTST)	150°C for 1000 hours

Table 4. WLCSP BOARD−LEVEL QUALIFICATION

Board Level	
Temperature	−40°C to 125°C for 2500 cycles with no failures

Mechanical Information and Circuit Design Guidelines

BelaSigna 300 AM is available in a 2.68 x 3.63 mm ultra−miniature wafer−level chip scale package (WLCSP)

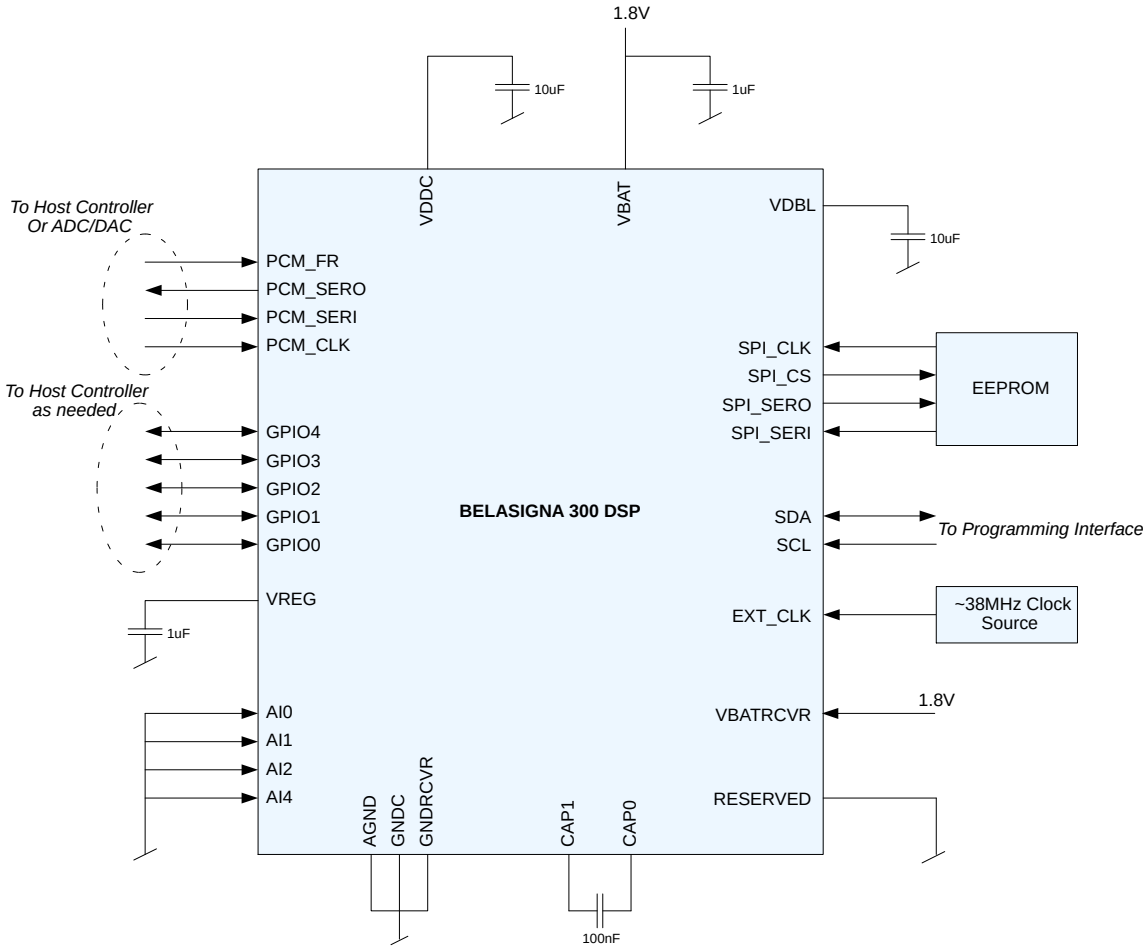


Figure 1. BelaSigna 300 with AfterMaster Layout Schematic

WLCSP Pin Out

A total of 35 active pins are present on the BelaSigna 300 AM WLCSP package. They are organized in a staggered array. A description of these pins is given in Table 5.

Table 5. WLCSP PAD DESCRIPTIONS

Pad Index	BelaSigna 300 AM Pad Name	Description	I/O	A/D
A1	GNDRCVR	Ground for output driver	N/A	A
A5	VBATRCVR	Power supply for output stage / NC for AfterMaster	I	A
B2	RCVR_HP+	Extra output driver pad for high power mode / NC for AfterMaster*	O	A
C3	RCVR+	Output from output driver / NC for AfterMaster*	O	A
A3	RCVR−	Output from output driver / NC for AfterMaster*	O	A
B4	RCVR_HP−	Extra output driver pad for high power mode / NC for AfterMaster*	O	A
B6	CAP0	Charge pump capacitor pin 0	N/A	A
C5	CAP1	Charge pump capacitor pin 1	N/A	A
A7	VDBL	Doubled voltage	O	A
B8	VBAT	Power supply	I	A
B10	VREG	Regulated supply voltage / NC for AfterMaster*	O	A
A9	AGND	Analog ground	N/A	A
A11	AI4	Audio signal input 4 / NC for AfterMaster*	I	A
B12	AI2/LOUT2	Audio signal input 2/output signal from preamp 2 / GND for AfterMaster*	I/O	A
A13	AI1/LOUT1	Audio signal input 1/output signal from preamp 1 / GND for AfterMaster*	I/O	A
B14	AI0/LOUT0	Audio signal input 0/output signal from preamp 0 / GND for AfterMaster*	I/O	A
D14	GPIO[4]/LSAD[4]	General−purpose I/O 4/low speed AD input 4	I/O	A/D
E13	GPIO[3]/LSAD[3]	General−purpose I/O 3/low speed AD input 3	I/O	A/D
C13	GPIO[2]/LSAD[2]	General−purpose I/O 2/low speed AD input 2	I/O	A/D
D12	GPIO[1]/LSAD[1]/UART−RX	General−purpose I/O 1/low speed AD input 1/and UART RX	I/O	A/D
E11	GPIO[0]/UART−TX	General−purpose I/O 0/UART TX	I/O	A/D
C9	GNDC	Digital ground	N/A	A
C11	SDA (I2C)	I2C data	I/O	D
D10	SCL (I2C)	I2C clock	I/O	D
E9	EXT_CLK	External clock input/internal clock output	I/O	D
D8	VDDC	Core logic power	O	A
E7	SPI_CLK	Serial peripheral interface clock	O	D
C7	SPI_SERI	Serial peripheral interface input	I	D
D6	SPI_CS	Serial peripheral interface chip select	O	D
E5	SPI_SERO	Serial peripheral interface output	O	D
D4	PCM_FR	PCM interface frame	I/O	D
E3	PCM_SERI	PCM interface input	I	D
D2	PCM_SERO	PCM interface output	O	D
C1	PCM_CLK	PCM interface clock	I/O	D
E1	Reserved	Reserved / GND for AfterMaster		

*NC = Not Connected.

WLCSP Assembly / Design Notes

For PCB manufacture with BelaSigna 300 AM WLCSP, ON Semiconductor recommends solder−on−pad (SoP) surface finish. With SoP, the solder mask opening should be non−solder mask−defined (NSMD) and copper pad geometry will be dictated by the PCB vendor's design requirements.

Alternative surface finishes are ENiG and OSP; volume of screened solder paste (#5) should be less than 0.0008 mm^3. If no pre−screening of solder paste is used, then following conditions must be met:

1. the solder mask opening should be >0.3 mm in diameter,
2. the copper pad will have 0.25 mm diameter, and
3. soldermask thickness should be less than 1 mil thick above the copper surface.

ON Semiconductor can provide BelaSigna 300 AM WLCSP land pattern CAD files to assist your PCB design upon request.

WLCSP Weight

BelaSigna 300 AM WLCSP (B300W35A109XXG) has an average weight of 0.095 grams.

Digital Interfaces

General−Purpose Input Output (GPIO) Ports

BelaSigna 300 AM has five GPIO ports that can connect to external digital inputs such as push buttons, or digital outputs such as the control or trigger of an external companion chip (GPIO[0..4]). The direction of these ports (input or output) is configurable and each pin has an internal pull−up resistor when configured as a GPIO. A read from an unconnected pin will give a value of logic 1. Four of the five GPIO pins are multiplexed with an LSAD (see the Low−Speed A.D Converters section) and as such the functionality of the pin can be either a GPIO or an LSAD depending on the configuration. Note that GPIO0 cannot be used as an LSAD.

Inter−IC Communication (I^2C) Interfaces

The I^2C interface is an industry−standard interface that can be used for high−speed transmission of data between BelaSigna 300 AM and an external device. The interface operates at speeds up to 400 Kbit/sec for system clocks (EXT_CLK) higher than 1.6 MHz. In product development mode, the I^2C interface is used for application debugging purposes, communicating with the BelaSigna 300 AM development tools. The interface can be configured to operate in either master mode or slave mode.

Serial Peripheral Interface (SPI) Port

An SPI port is available on BelaSigna 300 AM for applications such as communication with a non−volatile memory (EEPROM). The I/O levels on this port are defined by the VBAT. The SPI port operates in master mode only, which supports communications with slave SPI devices.

The SPI port on BelaSigna 300 AM only supports master mode, so it will only communicate with SPI slave devices. When connecting to an SPI slave device other than a boot EEPROM, the SPI_CS pin should be left unconnected and the slave device CS line should be driven from a GPIO to avoid BelaSigna 300 AM boot malfunction. When connecting to an SPI EEPROM for boot, the designer can choose to connect the SPI_CS pin to the EEPROM or use a GPIO (high at boot) for a design with several daisy-chained SPI devices.

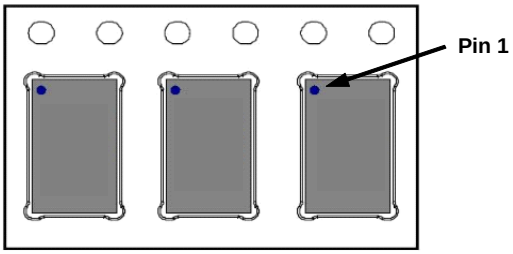
PCM Interface

BelaSigna 300 AM includes a highly configurable pulse code modulation (PCM) interface that can be used to stream audio signal data into and out of the device. The I/O levels on this port are defined by the voltage on the VBAT pin.

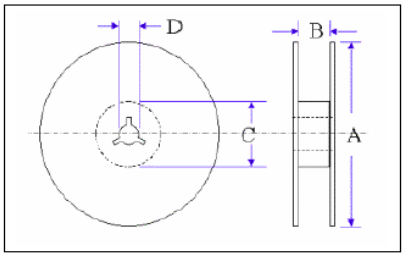
Assembly Information

CARRIER DETAILS
2.6 x 3.8 mm WLCSP

ON Semiconductor offers tape and reel packing for BelaSigna 300 AM WLCSP. The packing consists of a pocketed carrier tape, a cover tape, and a molded anti−static polystyrene reel. The carrier and cover tape create an ESD safe environment, protecting the components from physical and electrostatic damage during shipping and handling.

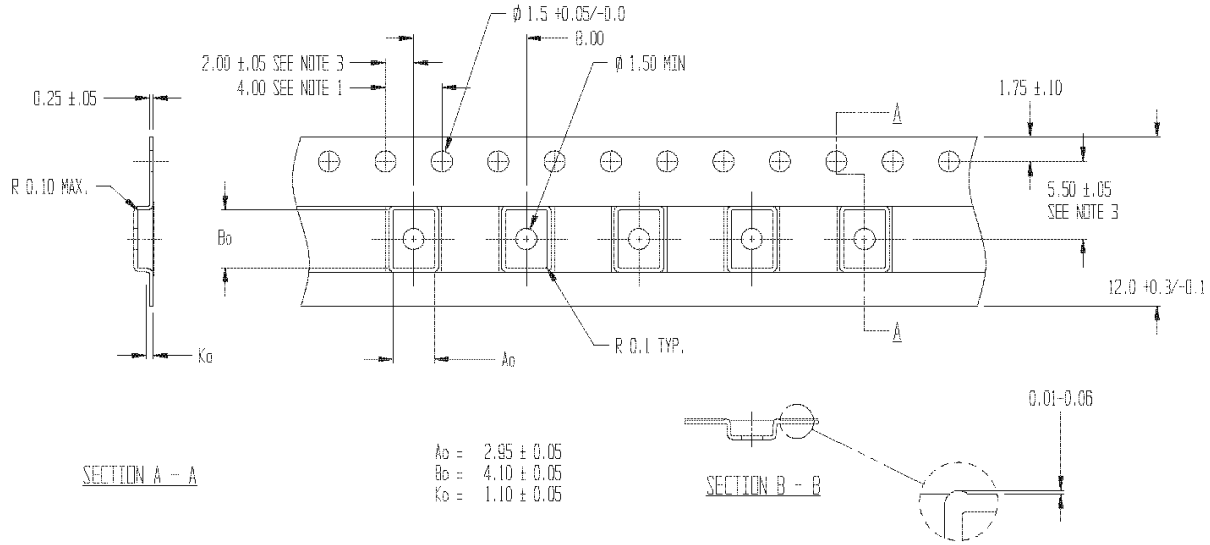


Quantity per Reel: 2500 units
Pin 1 Orientation: Upper Left, Bumps down
Tape Brand / Width: Advantek / 12 mm
Pocket Pitch: 8 mm
P/N: BCB043
Cover Tape: 3M 2666 PSA 9.3 mm



A = 13 inches
B = 12 mm
C = 4 inches
D = 13 mm
Reel Brand / Width: Advantek Lokreel® / 13 in

Figure 2. Package Orientation on Tape for WLCSP Package Option



10 sprockets hole pitch cumulative tolerance ±0.1.
Camber in compliance with EIA 763.
Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 3. WLCSP Carrier Tape Drawing

Sample Shipping Label



Figure 4. Sample Shipping Label

Re−Flow Information

The re−flow profile depends on the equipment that is used for the re−flow and the assembly that is being re−flowed. Information from JEDEC Standard 22−A113D and J−STD−020D.01 can be used as a guideline.

Electrostatic Discharge (ESD) Sensitive Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality. Device is 2 kV HBM ESD qualified.

Miscellaneous

Ordering Information

To order BelaSigna 300 with AM, please contact your account manager and ask for part number B300W35A109A1G.

Chip Identification

Chip identification information can be retrieved by using the Communications Accelerator Adaptor (CAA) tool along with the protocol software provided by ON Semiconductor (see CAA instruction manual). For BelaSigna 300 AM, the key identifier components and values are as follows for the different package options:

Package Option	Chip Family	Chip Version	Chip Revision
WLCSP	0x03	0x02	0x0100

Support Software

A set of tools is available at http://onsemi.com for downloading the proprietary AfterMaster HD algorithm to BelaSigna 300 AM. An AfterMaster HD image is supplied by ON Semiconductor, but must be downloaded to BelaSigna 300 AM upon boot.

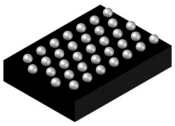
Training

To facilitate development on the BelaSigna 300 AM platform, training is available upon request. Contact your account manager for more information.

Company or Product Inquiries

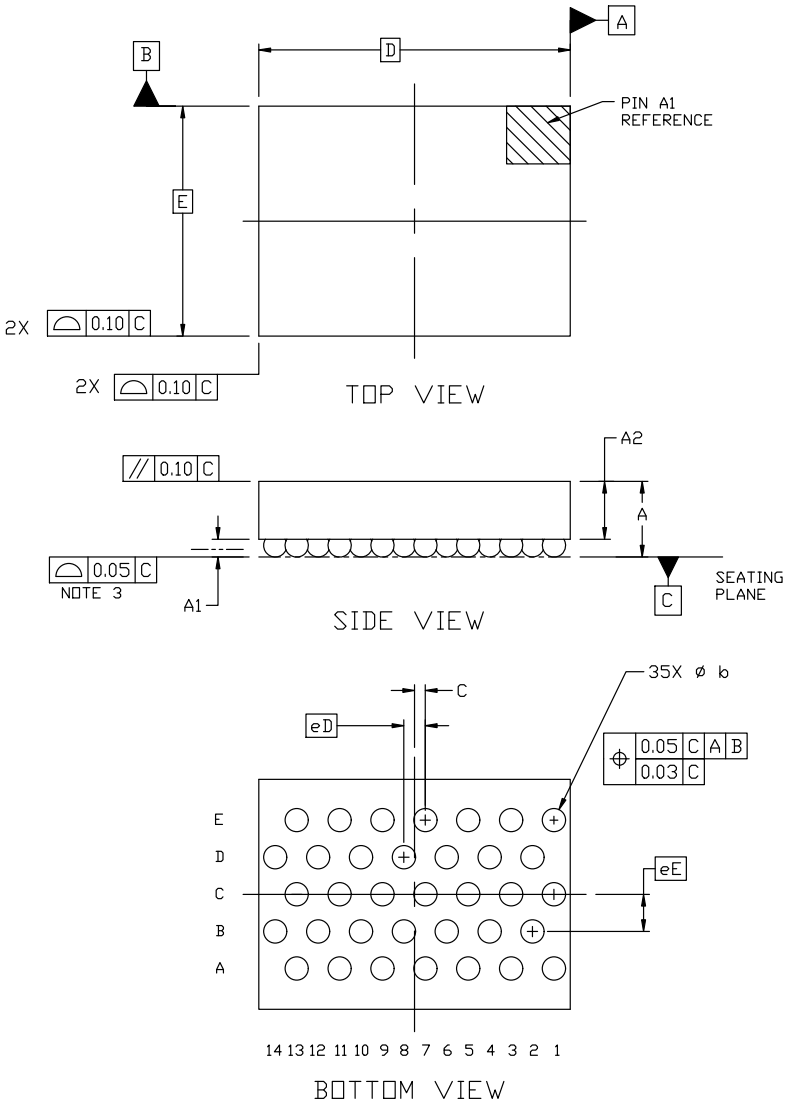
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WLCSP35, 3.63x2.68
CASE 567AG
ISSUE C

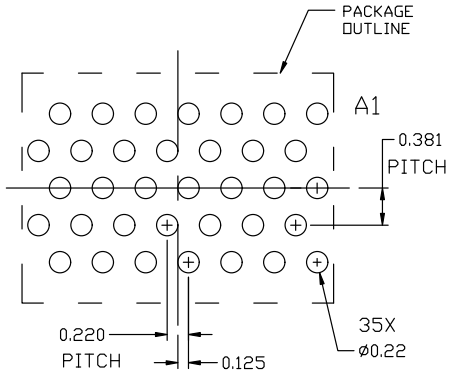
DATE 20 OCT 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.832	0.882	0.932
A1	0.182	0.207	0.232
A2	0.650	0.675	0.700
b	0.244	0.269	0.294
C	0.125 BSC		
D	3.633 BSC		
E	2.680 BSC		
eD	0.250 BSC		
eE	0.433 BSC		



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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